Energy harvesting applications for Low Voltage Dynamic CTS CMOS Charge Pump

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Abstract*—This paper brings a detailed analysis and comparison of several charge pumps topologies that have not been optimized yet in order to make a relevant comparison of main parameters. The charge pumps were designed in a standard 90nm CMOS technology. Highly efficient CMOS charge pump which is designed using charge transfer switches. The circuit provides higher output voltage then existing ones. This is achieved by replacing diode with charge transfer block at the last stage of dynamic CTS charge pump. This eliminates threshold voltage loss, leakage current, and body effect problem. The charge pump are designed in a standard CMOS technology which Provides the superior pumping efficiency, settling time, ON-chip power management and voltage gain. The proposed circuit is designed and simulated using T-spice and H-spice with CMOS technology parameters.*

I. INTRODUCTION

The charge pump is a dc-dc converting circuit used to obtain a dc voltage higher or lower than the supply voltage or opposite in polarity to the supply voltage. Charge pump circuits use capacitors as energy storage devices. The capacitors are switched in such a way that the desired voltage conversion occurs. Charge pumps are useful in many different types of circuits, including low-voltage circuits, dynamic random access memory circuits, switched-capacitor circuits, EEPROM's and transceivers.

The proliferation of portable, battery-operated electronic systems has increased the need for highly efficient, low-voltage-capable DC-DC boost converters. Emerging niche classes of wireless sensor-based electronic products such as smart sensors, biomedical implants, etc., [2] necessitate power-autonomy to provide essential operation for several years without the need for battery replacement. In these systems, power-autonomy is realized by harvesting or scavenging energy from the surroundings using transducers such as thermoelectric generators (TEG), photovoltaic cells (PV) and piezoelectric sensors. Due to variations in the operating conditions, these transducers do not generate a constant output. Hence, energy harvesters employ power management circuits (PMC) to optimize the conversion efficiency.

II. DICKSON CHARGE PUMP

The Dickson charge pump circuit is basically a DC to DC boost converter. Which provides high output even low input voltage. In the Dickson charge pump circuit, the coupling capacitors are connected in parallel and must be able to withstand the full output voltage. This results in a lower output impedance as the number of stages increases. The drawback of the Dickson charge pump circuit is that the boosting ratio is 3 degraded by the threshold drops across the diodes. The body effect makes this problem even worse at higher voltages. Dickson charge pump circuits where diodes are used as switches and can be implemented with diode connected MOSFETs [6].

One of most commonly used voltage multipliers is Dickson Charge pump in which diode-connected NMOS is used as charge transfer device as shown in Fig. 1. The voltage gain of each stage in Dickson charge pump, which is defined as the difference between the output and input voltages of this stage, is given by:

$$Gv = V - V_{tn} \quad (1)$$

Where V_{tn} is the threshold voltage of the diode-connected NMOS modified by the body effect due to source voltage increasing at each stage. _V is the voltage fluctuation at each pumping node [11] to obtain a positive voltage step in each stage. Therefore, Dickson charge pump is not properly suitable for low-voltage applications.

Many modifications to the Dickson charge pump have been proposed to enable it to operate at low input voltage levels. for example, the diode voltage drop is eliminated by using charge transfer switch (CTS) in parallel with the diode connected device in order to improve the performance in low voltage applications. Static and dynamic CTS techniques.

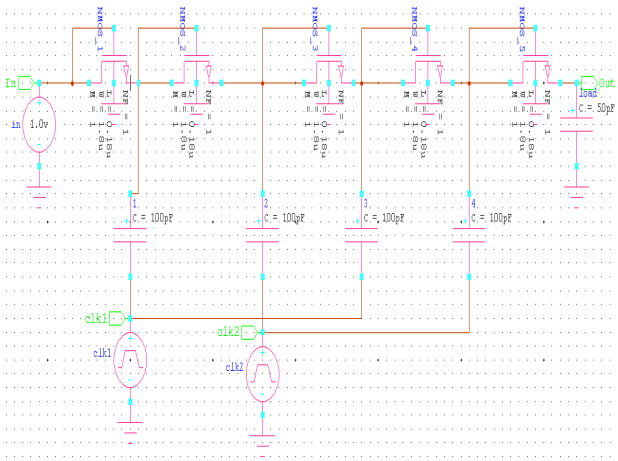


Fig. 1 Basic Dickson charge pump

III. PROPOSED FRAMEWORK

The purposed improved charge transfer switch charge

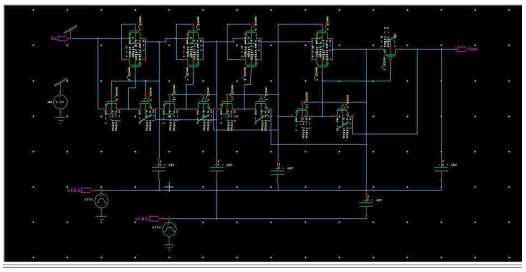


Fig. 2 proposed charge transfer switch CMOS charge pump

pump eliminates the major disadvantage of basic charge transfer switches in which NMOS were not completely turn off so due to this reverse current flows, which will reduces the overall voltage gain. So in this proposed charge pump pass transistors are used to reduce this effect. This charge pump has many RFID applications

Our proposed 4-stage improved dynamic CTS CP, based on the combination of the dynamic CTS CP and auxiliary MOSFETs at the last stage. This circuit employs dynamic charge transfer switches. Each of the CTS (MSs Transistor) is controlled by the pass transistor MNs and MPs.

The dynamic CTSs are used to transfer charges from one stage to the next without suffering the problem of V_{TH} voltage drop. As shown in Fig. 1, pass transistors MNs and MPs have been used to dynamically control the inputs for the CTSs so that they can be turned off completely when required. At the same time they can be turned on easily by the feedback control mechanism. To boost the charge, both the clock signals CLK 1 and CLK2 are out-of-phase but with the amplitudes of VIN. The MOSFET MS1 is connected in parallel to MOS-diode MD1. MN1 and MP1 transistors are added such that MS1 is completely ON when MD1 is ON and MS1 is completely OFF if MD1 is OFF.

As the clk1 goes low and clk2 goes high. The voltage at node one is Vin. The voltage at node 2 become greater then node one. Makes MP1 turned on and MN1 of as Vgs=0. The NMOS MS1 conducts and the output at node one become Vin

Similarly at time T2 when clk 1 goes high and clk2 goes low the MP1 become completely turned off as Vgs=0. The voltage at node one becomes greater then the voltage at node 2.it makes MN1 on. Diode MS1 completely off. Reverse charge flow is avoided. The same process occurs for the other stages as well In the simple dynamic charge transfer switches cmos charge pumps MD0 diode is used at the output. MD0 is NMOS implemented as the output increases nadal voltage of MD0 also increases. Resulting in the increase of threshold voltage resulting loss in the output voltage

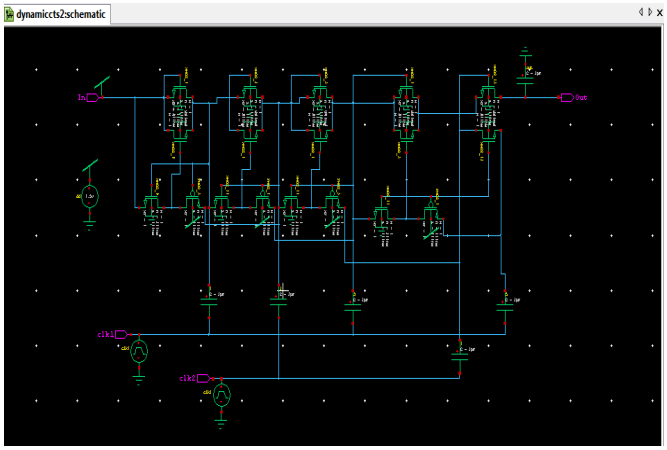


Fig. 3 dynamic CMOS charge pump

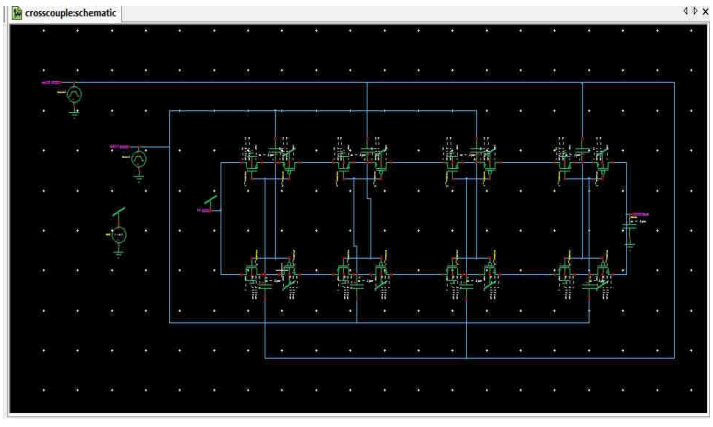


Fig. 4 cross couple charge pump

the body of M1 are connected through M3 and no reverse bias exists between the source and the body of the charge-transfer MOSFET, preventing threshold voltage increase due to body effect. Next, if M1 is OFF, M2 turns ON. Then the drain and the body of the charge-transfer MOSFET are connected through M2, to prevent the body from floating. The body voltage of M1 keeps track of lower value of the source or the drain voltage at each clock state by the auxiliary MOSFETs. This helps to minimize body effect loss. The capacitor C is used to smooth the voltage fluctuation at the output.

IV. SIMULATION AND RESULTS

The improved dynamic CTS charge pump has been designed and simulated using T-spice and H-Spice, 0.18µm technology. All the simulations are carried out at 500MHz and with MOSFETs of same size (W/L=240nm/180nm). And PMOS (W/L=480nm/180nm), NMOS in driving circuitry (auxiliary MOSFET block) (W/L=960nm/180nm). Amplitude of CLK1 and CLK2 are same as the input voltage (VIN).

Fig. shows the simulated output voltage of this improved charge pump circuit for varying input voltage (Vin) from 1.5v to 0.6v

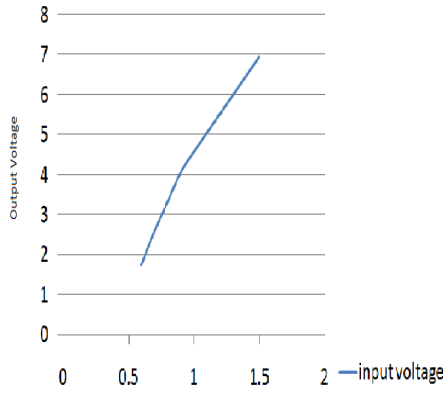


Fig 5.4.1 plot between varying input voltage and increasing output voltage gain of improved dynamic CTS CMOS charge pump

In improved dynamic CTS CMOS charge pump as the value of the load resistance increases the output voltage of the system also increases. Load resistance varies from 100k to 1G w.r.t to it voltage gain is increased upto 4.77v at the constant supply of 1.0v .as increasing the load resistance the performance parameters are improving.

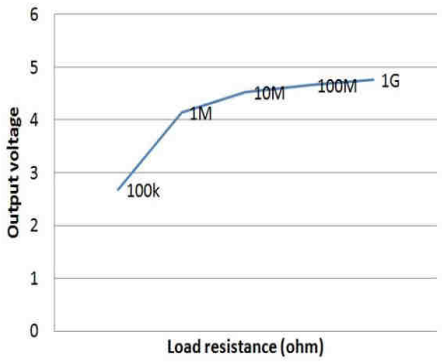
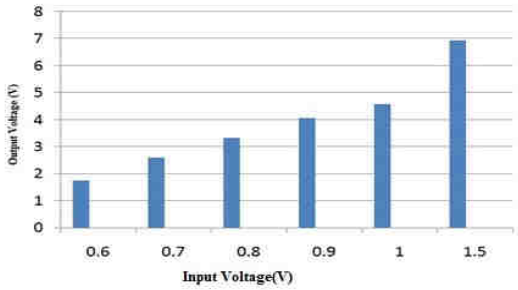


Fig 5.4.2 plot between load resistance and the output voltage improved dynamic CTS CMOS charge pump



5.4.3 Output Voltage chart for Improved CTS CMOS charge pump with varying input voltage

Table 1. Performance Parameters of 4-Stage improved CTS Charge Pump

Supply Voltage	Average Power Consumption (µW)	Settling Time (µs)	Output Voltage (V)	Pumping Efficiency (%)
1.5V	40.62	1.97	5.94	90.5
1.0	16.47	4.37	4.57	89.2
0.9	12.99	5.48	3.06	87
0.8	10.86	6.32	3.32	82.75
0.7	7.46	7.34	2.59	70.7
0.6	5.57	8.61	1.75	58.33

Table 2. Performance Parameters of 4-Stage improved CTS Charge Pump for variation of load resistance

Load Resistance (Ω)	Average Power Consumption (µW)	Settling Time (µs)	Output Voltage (V)
100K	112.37	9.95	2.69
1.0 M	32.84	1.22	4.15
10M	16.24	0.929	4.53
100M	15.79	0.907	4.67
1G	15.59	0.909	4.77

V. CONCLUSION & FUTURE WORK

An improved dynamic CTS charge pump has been realized by controlling the body voltage of MOS at the last stage of the dynamic CTS CP. This is achieved by adding auxiliary MOS at the last stage of dynamic CTS charge pump to remove the threshold voltage increase. The proposed circuit compared to Dynamic CTS CP, provides a considerable increase of output for an input voltage up to 4 stages. Optimum transistor sizing plays a very important role in design of CMOS logic circuits. In this design, we have focused on keeping optimum design for low power applications. For input voltages greater than or equal to 0.6 V, the proposed circuit gives higher output voltages than dynamic CTS CP. A considerable amount of 0.5V increase in the output voltage matters a lot in low power energy harvesting applications.

CMOS charge pumps are basically dc-to-dc converters used to convert low input voltage to high output voltage. Mostly used charge pumps are based on Dickson charge pump having various limitations such as reverse current, body effect problem, increasing threshold voltage. The proposed work eliminates all these limitations providing better results such as output gain, settling time, efficiency etc. up to very low voltage. This design provides the superior results among all existing architectures. This work can be further improved by incorporating new circuit topologies minimizing the problem of body effect and increasing threshold voltage. As technology is changing day by day several improvements can be made for improving voltage output gain and for improving efficiency for low voltage applications. Lot of research can be carried out to increase the pumping efficiency at lower input voltages i.e. below 0.5V.

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