An Efficient Baugh-Wooley Multiplication Algorithm for 32-bit Synchronous Multiplication

Rakesh Kumar, Pradeep Kumar

ABSTRACT:
This paper presents an efficient implementation of a high speed 32-bit synchronous Baugh-Wooley multiplier using the Brent-Kung. BW multiplier involves basic operations of generation of partial product and their accumulation. As a result of which they occupy less area and provides fast speed as compared to the serial multiplier. This is very important criteria because in the fabrication of chips and high performance system requires components which are as small as possible. Experimental result demonstrates that the proposed multiplication algorithm not only improves the accurate performance but also improves the speed of multiplication. The array structure of Synchronous Baugh-Wooley Multiplier is obtained from RTL synthesis is shown. Different parameters like CPU usage, power, area and memory usage has been compared.

Keywords: Multipliers, Brent-Kung, Fabrication, Synchronous Baugh-Wooley

I. INTRODUCTION:

Day by day a faster design with smaller area and lower power consumption is essential for the modern electronic designs [1]. In microelectronics design multiplier is a fundamental unit and widely used in circuits, for which the multiplication process should be optimized properly. Multipliers generally have extended latency, huge area and consume substantial amount of power. Hence designing of low-power multiplier has become an important part in VLSI system design [5]. So in our project we have tried to design a faster full width synchronous multiplier that computes the 2n output as a weighted sum of partial products using BK adder [8]. Thus the main aim of this project to design a 32-bit synchronous BW multiplier and reduction of area, delay and size of the multiplier.

II. BAUGH-WOOLEY TWO'S COMPLIMENT SIGNED & UNSIGNED MULTIPLICATION:

Baugh-Wooley Two's compliment Signed multipliers is the best known algorithm for signed multiplication because it maximizes the linearity of the multiplier and allow all the partial products to have positive sign bits [10]. Baugh–Wooley technique was developed to design direct multipliers for Two's compliment numbers. When multiplying two's compliment numbers directly, each of the partial products to be added is a sign number. Thus each partial product has to be sign extended to the width of the final product in order to form a correct sum by the Carry Save Adder (CSA) tree. According to Baugh-Wooley approach, an efficient method of adding extra entries to the bit matrix suggested to avoid having deal with the negatively weighted bits in the partial product matrix. In figure 1 (a) & (b) partial product arrays of 5*5 bits Unsigned and Signed bits are shown:

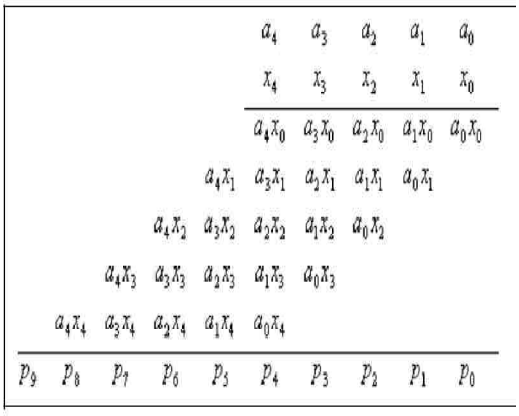

Figure 1 (a): 5*5 unsigned multiplication [10]

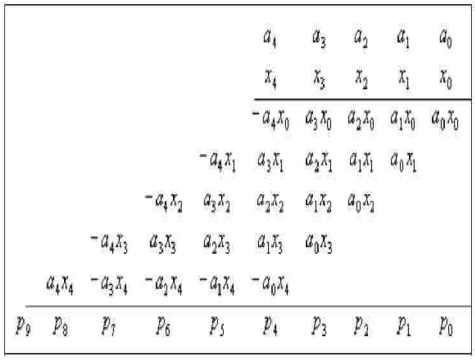

Figure 1 (b): 5*5 Signed multiplication [10]

Figure 1 (c) shows how Baugh-Wooley algorithm works in the case of a 5x5 multiplication. The first three rows are referred to as PM (partial products with magnitude) and generated by one NAND and three AND operations. Fourth row is called as PS (partial products with sign bit) and generated by one AND and three NAND operations with a sign bit. Considering the partial products of PM, suppose b2= b0 in figure1 (c). Then the third row can be obtained by shifting the first row by 2 bits. Likewise, shift operation can be used to obtain a partial product of different bit level as in sign magnitude multiplication.

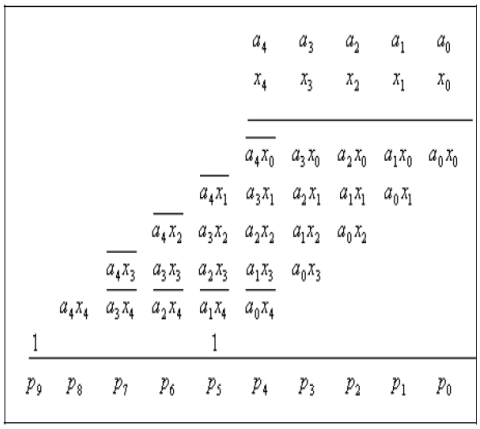

Figure 1 (c): 5*5 Multiplication Example of Baugh-Wooley Algorithm [10]

III. BAUGH-WOOLEY MULTIPLICATION USING BK ADDER

The Brent-Kung adder is a parallel prefix adder. Parallel prefix adders are special class of adders that are based on the generation and propagation of signals. Simpler Brent- Kung adders were proposed to solve the disadvantages of Kogge-Stone adders. The wiring complexity and cost is greatly reduced. But the logic depth of BK adders increases to 2log (2n-1), so the speed is lower. The block diagram of 4-bit Brent-Kung adder is shown in figure 2.

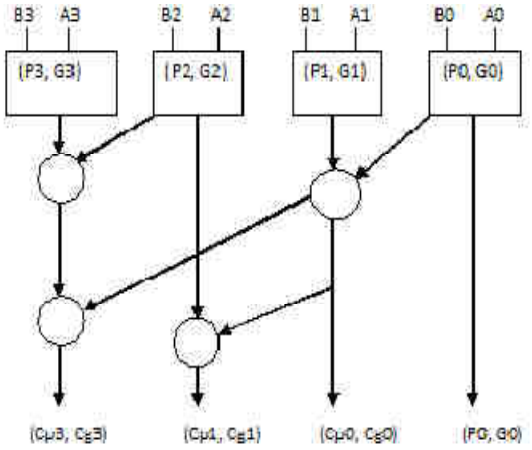

Figure 2: 4 -bit Brent-Kung adder [8]

BW Multiplication involves two basic operations: (a) Generation of the partial product (b) and their accumulation. Therefore, there are possible ways to speed up the multiplication: reduces the complexity, and as a result reduces the time needed to accumulate the partial products.

Brent-Kung adder (BK adder) is an advanced design prefix adder, which is a very good balance between area and power cost and also it will present better performance. BK adder has a complex carry and inverse carry tree. A tree can be divided into 2 types that are a tree and an inverse tree. Upper tree is based on periodic power of 2.

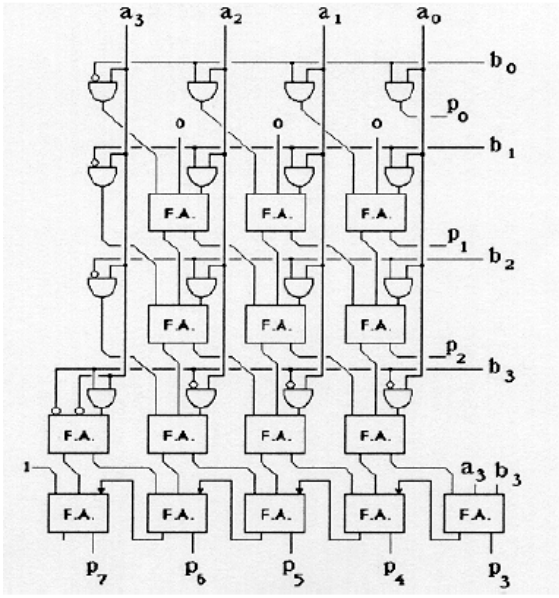

Figure 3: Architecture of Baugh-Wooley Multiplier [9]

IV. SYNTHESIS RESULTS & IMPLEMENTATION:

In this project I have done the coding in VHDL of Baugh-Wooley algorithm for both synchronous and asynchronous multiplication. The VHDL codes synthesized on Xilinx ISE 8.1 and simulated using Xilinx ISE simulator. Output simulation, device utilization and timing summary obtained from synthesis report are used to compare both multipliers. As LUTs are proportional to the area occupied by the multipliers on VLSI chip and path delay is inversely proportional to the speed of the multiplier. These coding are also written in VHDL language and simulate it to get the RTL circuit of each system. Also get the lookup table, where we get the exact no of inputs, outputs and no of slices requirement etc for the system. Xilinx Power Estimator is used to determine the power consumption of the system. These results of multipliers are given below.

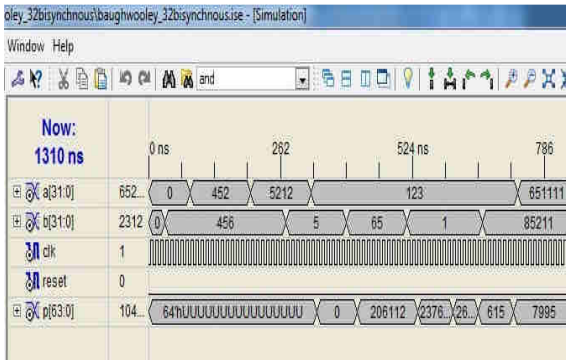

Figure 4: output simulation of 32-bit synchronous Baugh-Wooley multiplier

Table1. Synthesis report of asynchronous 32-bit BW multiplier

Device utilization summary (estimated values)			
Logic utilization	Used	Available	Utilization
Number of Slices	1037	10752	9%
Number of 4 input LUTs	2041	21504	9%
Number of bonded IOBs	128	448	28%

Maximum combination path delay: 48.09 ns

Table2. Synthesis report of synchronous 32-bit BW multiplier

Device utilization summary (estimated values)			
Logic utilization	Used	Available	Utilization
Number of Slices	2254	10752	20%
Number of 4 input LUTs	2130	21504	9%
Number of bonded IOBs	130	448	29%

Maximum combination path delay: 6.496 ns

V. CONCLUSION:

In this paper, a synchronous multiplier for 32 bit multiplication proposed in which partial products is generated using BK adder. The Output simulation and device utilization

summary obtained from synthesis report, shows that asynchronous BW has less number of LUTs as compare to synchronous multiplier but synchronous multiplier is fast in speed as compared to asynchronous multiplier. By simulating from synthesis we found that Maximum combinational path delay in this multiplier is 6.496ns, which is very effective and less as compare to other multipliers. This technique performs the multiplication of 32 bit. When we compare the path delay and area of synchronous BW multiplier with other multipliers, we found that synchronous multiplier using BK adder is better than other multipliers in terms of speed and area. So by using synchronous Baugh-Wooley multiplier using BK adder we can achieve the fast and efficient multiplication.

REFRENCES

[1] Anand Kumar., "*Fundamentals of Digital Circuits*", *Prentice Hall of India*, 2008.

[2] Manish Chaudhary, Mandeep Singh Narula., " *FPGA Implementation of Booth's and Baugh-wooley multiplier Using Verilog*" in International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-3, Issue-1, June 2013

[3] A. D. Booth "*A signed binary multiplication technique*," Quart. J. Mech. Appl. Math., vol.4

[4] Sukhmeetkaur, suman and manpreetsignh manna., "*Implementation of Modified Booth Algorithm (Radix 4) andits Comparison with Booth Algorithm (Radix-2)*" in Advance in Electronic and Electric Engineering. ISSN 2231-1297, Volume 3, Number 6 (2013), pp. 683-690

[5] Vikram Singh, Manish kumarjain., " *Estimation of Speed and Area of High Speed Multiplier Designed using Booth-Wallace Unit Add Method*" in International Journal of Scientific & Engineering Research, Volume 4, Issue 7, July 2013

[6] C. S. Wallace., "*A Suggestion for a Fast Multiplier*", *in IEEE Trans. on Electronic Computers*, vol. 13, pp. 14-17, 1964.

[7]. Morris Mano,,Digital Design, Third edition', "*Prentice Hall of India"*, 2000.

[8] AdilakshmiSiliveru, M.Bharathi., "*Design of Kogge-Stone and Brent-Kung adders using Degenerate Pass Transistor Logic*" in International Journal of Emerging Science and Engineering (IJESE) ISSN: 2319–6378, Volume-1, Issue-4, February 2013

[9]IndrayaniPatle, AkanshaBhargav, PrashantWanjari., "*Implementation of Baugh-Wooley Multiplier Based on Soft-core Processor*" in IOSR Journal of Engineering (IOSRJEN) e-ISSN: 2250-3021, p-ISSN: 2278-8719 Vol. 3, Issue 10 (October. 2013), ||V3|| PP 01-07

[10] PramodiniMohanty, RashmiRanjan, "*An Efficient Baugh-Wooley Architecture for both Signed & Unsigned Multiplication"* in International Journal of Computer Science & Engineering Technology (IJCSET), ISSN: 2229-3345, Vol. 3 No. 4, April 2012