Design of Low Power CMOS Level Shifter and Barrel Shifter

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Abstract—*With the developing interest of handheld gadgets like mobile phones, mixed media gadgets, individual note pads and so on., low power utilization has ended up significant configuration thought for VLSI circuits and framework. With expansion in force utilization, unwavering quality issue likewise rises and cost of bundling goes high. Power utilization in VLSI circuit comprises of dynamic and static force utilization. Dynamic force has two parts i.e. changing force because of the charging and releasing of the heap capacitance and the short out force because of the non-zero ascent and fall time of the information waveforms. The static force of CMOS circuits is dictated by the spillage current through every transistor. In System on chip (SoC) plan, diverse parts like advanced, simple, inactive segment are created on a solitary chip and needs distinctive voltages to accomplish ideal execution. A level shifter is typically a section that proselytes computerized signals starting with one rationale standard then onto the next. Level converters are utilized to change over the rationale signal from one voltage level to other level and are the noteworthy circuit segment in VLSI frameworks. Level shifters are likewise essential circuit segment in multi voltage frameworks and have been utilized as a part of between center circuits and I/O circuit. Barrel Shifter assumes an imperative part in the information moving and information revolution. It is having application in numerous regions. The Barrel Shifter is for the most part use for the rearrangements of the information moving. The Arithmetic and the Logical Shifters can likewise be supplanted by the Barrel Shifter Because with the turn of the information it additionally give the application the information right, left moving either numerically or sensibly. In this anticipate low power CMOS level shifter and 4bit barrel shifter are to be composed by utilizing different foundry advancements and thought about, the ideal one will be proposed.*

Keywords— SoC, CMOS level shifter, low power.

I. INTRODUCTION

High power scattering additionally prompts the decreased time of operation, higher weight because of batteries, lessened portability, cooling cost and diminished dependability. Battery life time relies on upon the interim amongst charging and framework cost. Since the gadget temperature increments because of high thickness of transistors, the disappointment rate, cooling and pressing expenses are the purposes behind the low power advanced VLSI plan. Additionally, it irritates the earth as warmth, it turns into a noteworthy issue now-a-days .

Level shifters are utilized as a part of multivdd configuration, Since in multivdd outline distinctive squares are taking a shot at various voltages. So when a sign goes starting with one voltage area then onto the next voltage space the level shifter is required especially when a sign goes from low voltage area to high voltage area.The level shifter will change over one voltage level from to another voltage.

A barrel shifter is a computerized circuit that can move an information word by a predetermined number of bits in one clock cycle. It can be executed as a succession of multiplexers (mux.), and in such a usage the yield of one mux is associated with the contribution of the following mux in a way that relies on upon the movement separation.

II. IMPLEMENTATION

Barrel shifters: We actualize a 4 bit barrel shifter which is a circuit will move the 4 bit information to the privilege or left relies on upon the data connected to the control inputs. In this way, clearly this circuit requests the utilization of multiplexer . A 4-1 multiplexer along withthe proper associations are utilized to manufacture a 4 bit barrel shifter. Barrel shifters are assuming a pivotal part in the chip focal handling unit while performing number juggling, rationale or roundabout method of operations for a given assignment .

Here, we utilize 4-1 multiplexer for the configuration of barrel shifter . 4-1 multiplexer can be actualized utilizing diverse CMOS rationale styles and the best one will be recognized by method for low power scattering, less format region and superior.

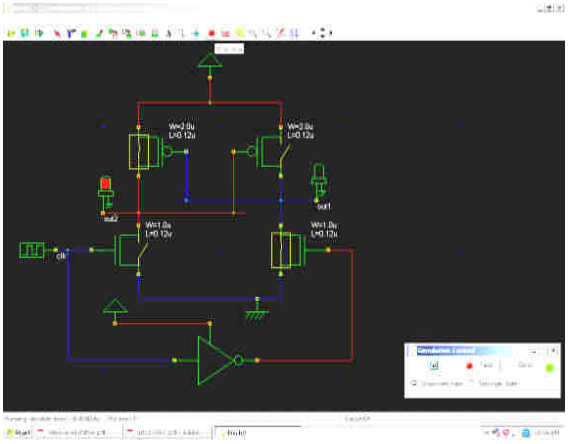

Fig.1: Conventional level shifter

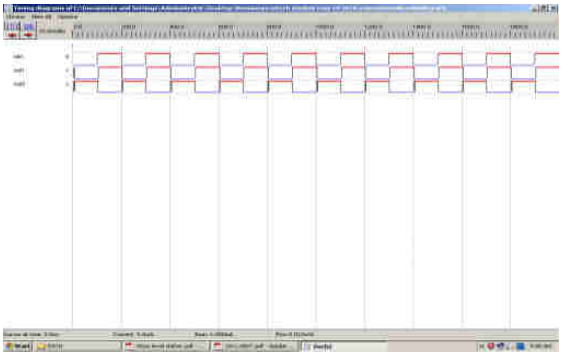

Fig.2: Analog waveform

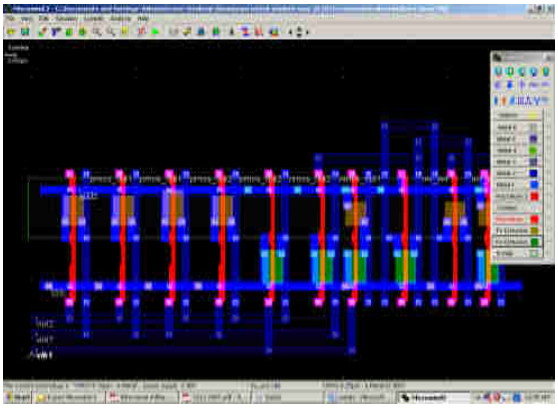

Fig.3: Layout for Conventional level shifter in 250nm

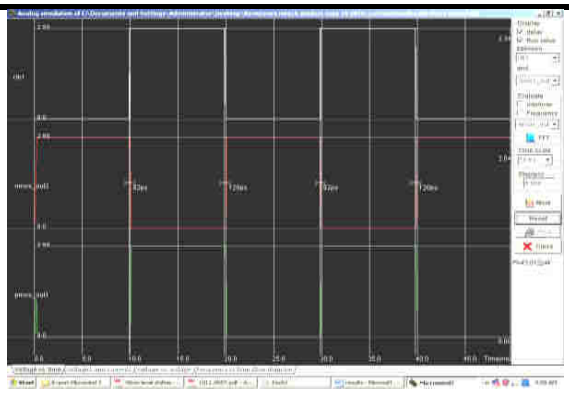

Fig.4: Conventional level shifter in 250nm technology

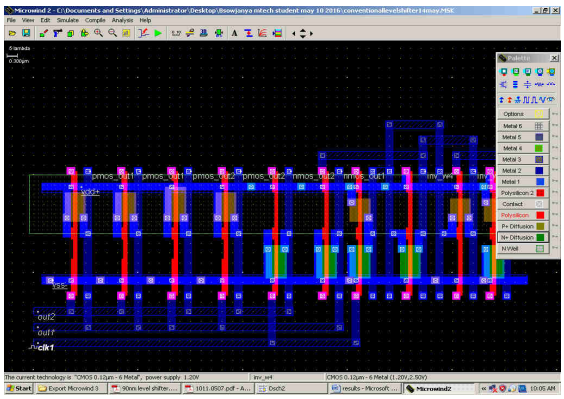

Fig.5: Layout for 120nm

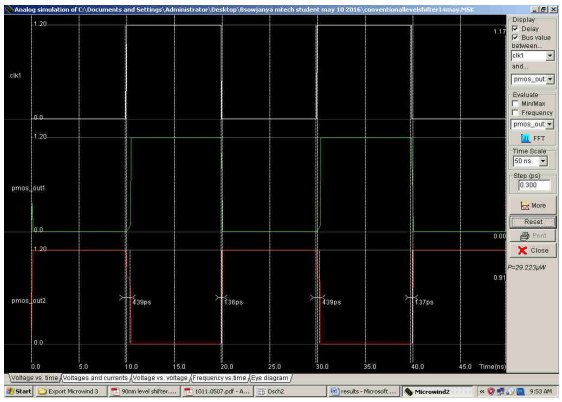

Fig.6: 120nm technology waveform

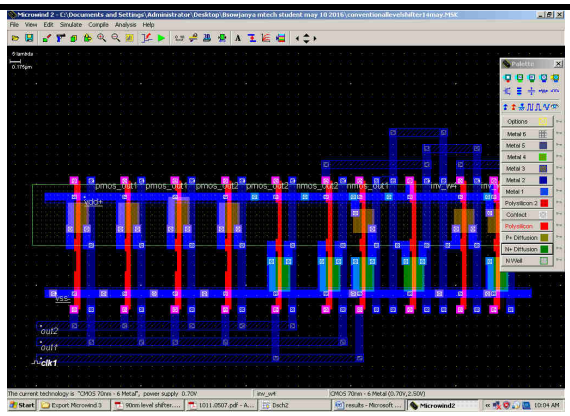

Fig.7: Layout 70nm

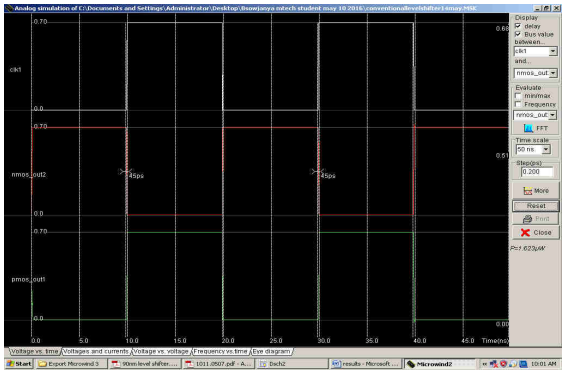

Fig.8 :70nm technology waveform

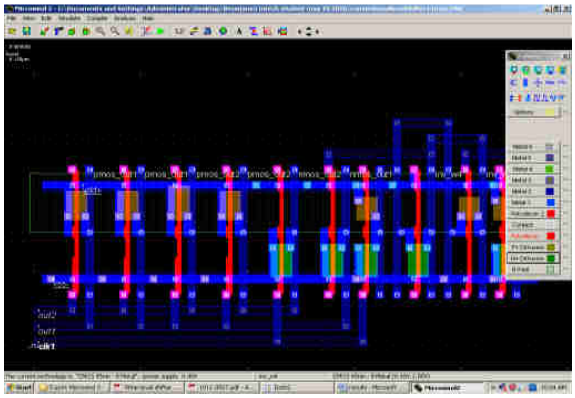

Fig.9: Layout 45nm

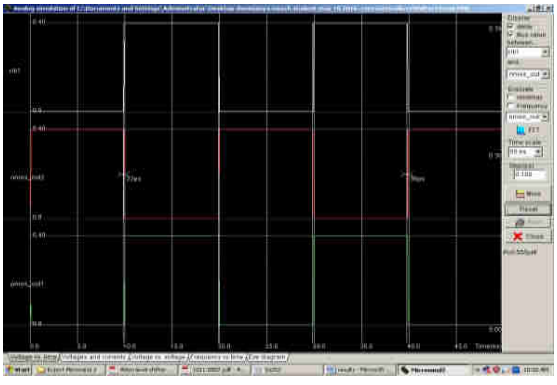

Fig.10: 45nm technology waveform

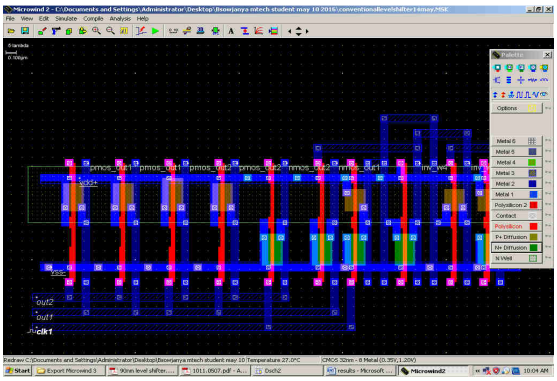

Fig.11: Layout32 nm

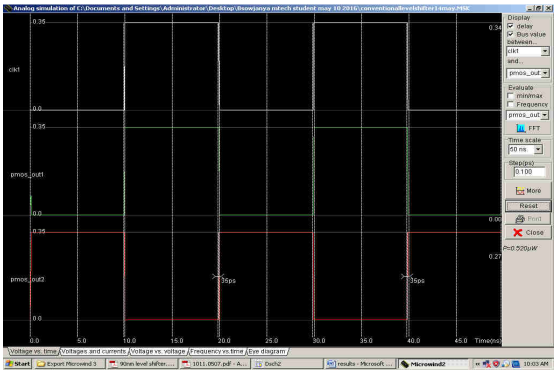

Fig.12: 32nm technology waveform

Table 1

SL. NO	FOUNDRY TECHNOLOGY(nm)	VOLTAGE (volts)	POWER DISSIPATION(µW)
1	250	2.5-2.30	43.012
2	120	1.20-2.5	29.232
3	70	0.7-2.5	1.623
4	45	0.4-1.8	0.55
5	32	0.35-1.2	0.52

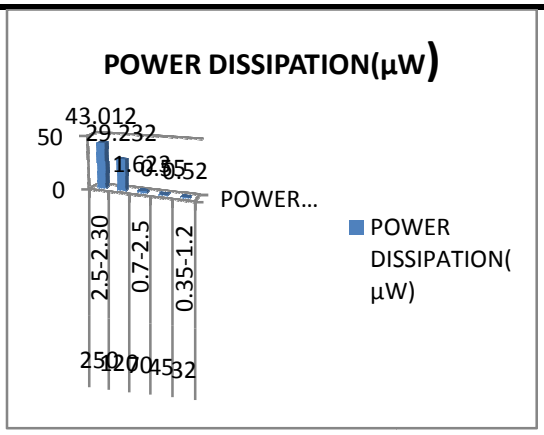

Fig.13: graph for different foundry technologies vs power dissipation

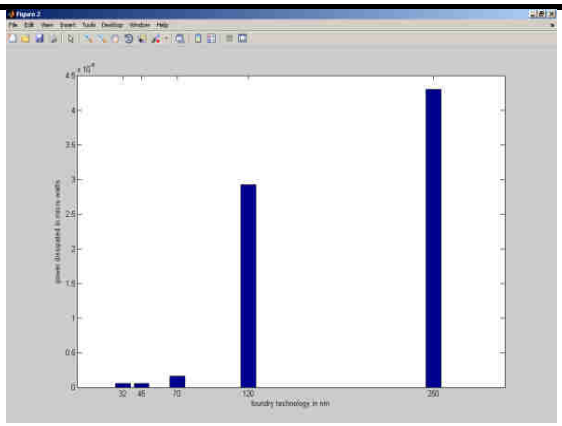

Fig.15: bargraph drawn for different foundry technologies vs power dissipation

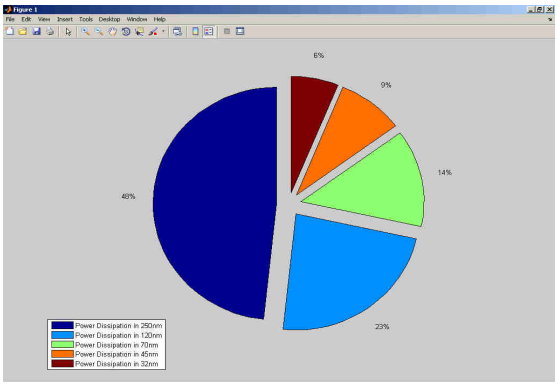

Fig.14: pie graph drawn for different foundry technologies vs power dissipation

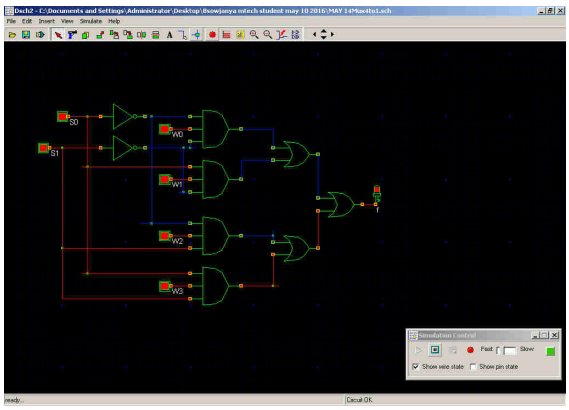

Fig.16: 4 BIT MUX DESIGN

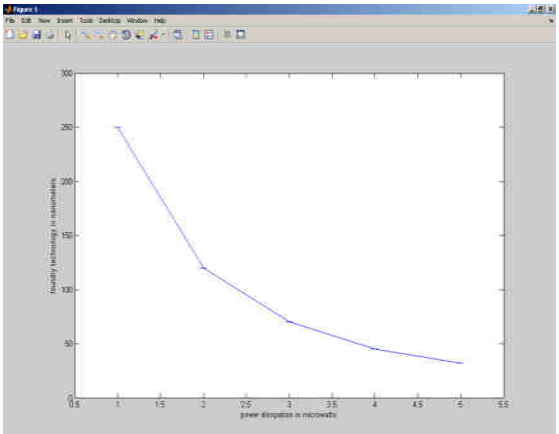

Fig.15: linear graph drawn for different foundry technologies vs power dissipation

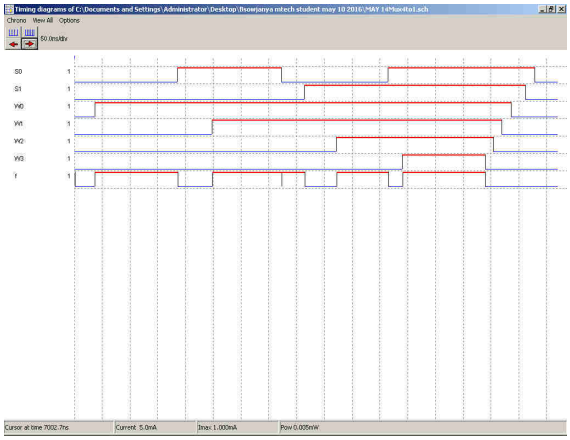

Fig.17:Analog waveforms

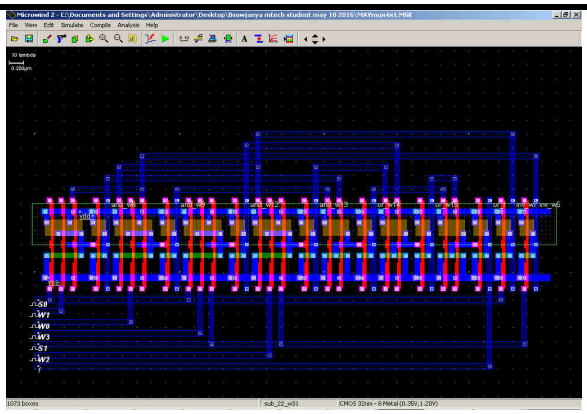

Fig.18:Layout of 4 BIT MUX

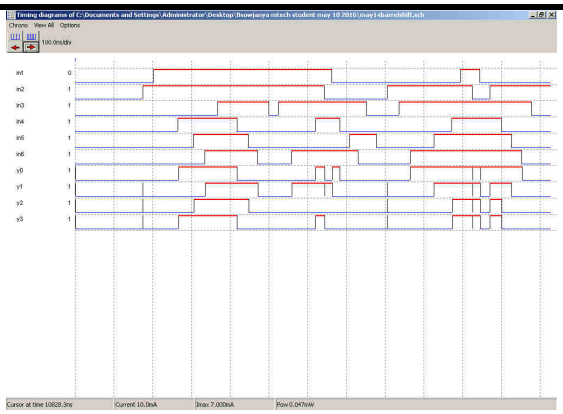

Fig.21:Analog waveforms

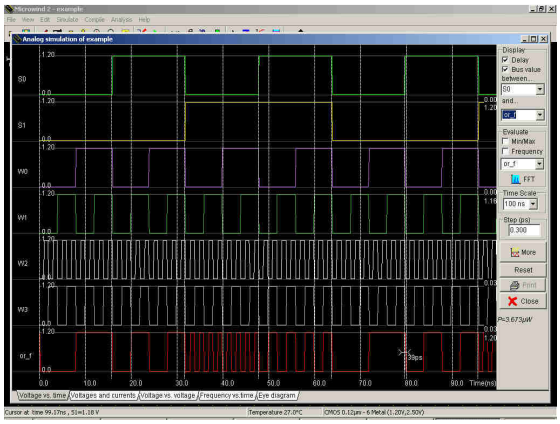

Fig.19: 4 BIT MUX waveforms

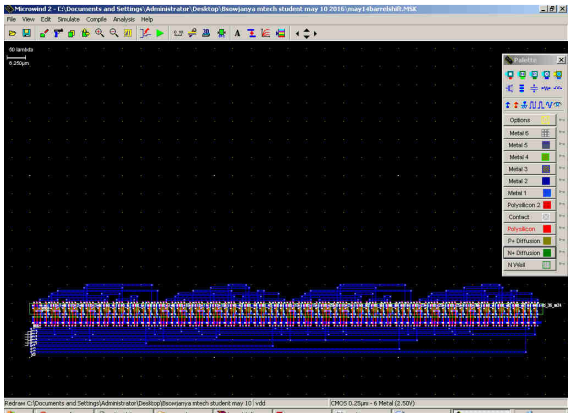

Fig.22: Layout 250nm

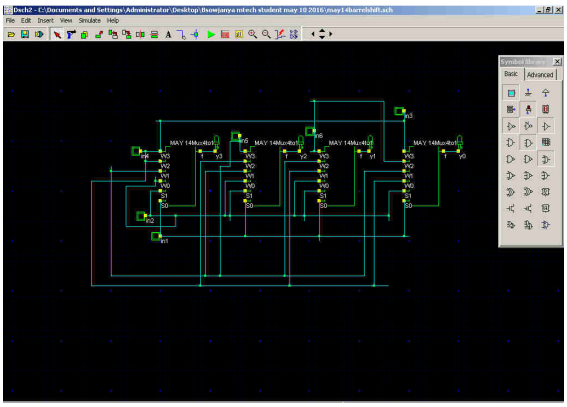

Fig.20: 4x1 barrel shifter using MUX

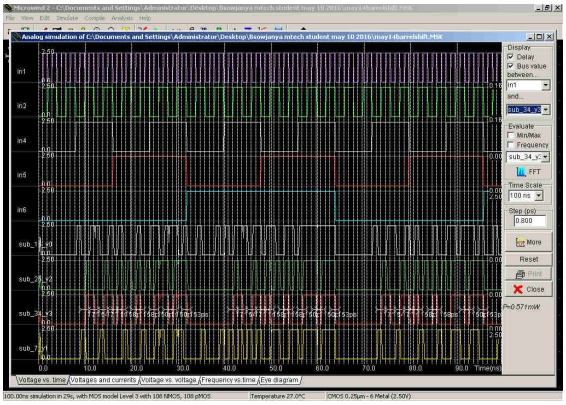

Fig.23: 250nm technology waveform

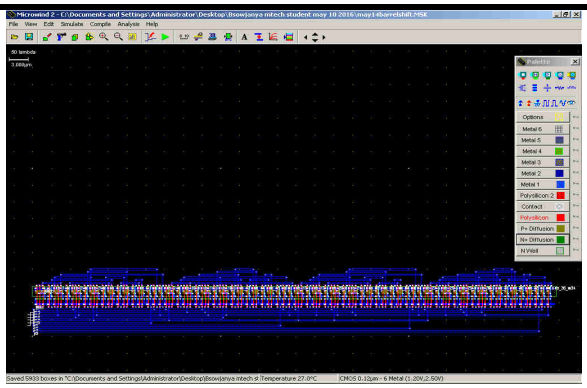

Fig.24:Layout 120nm

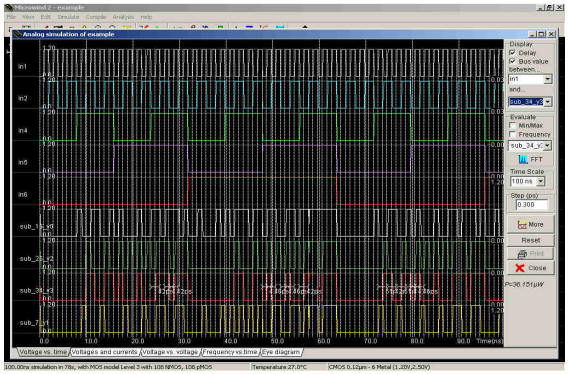

Fig.25:120nm Technology Waveforms

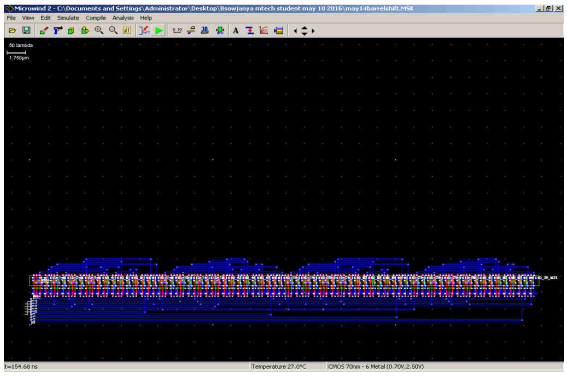

Fig.26:Layout 70nm

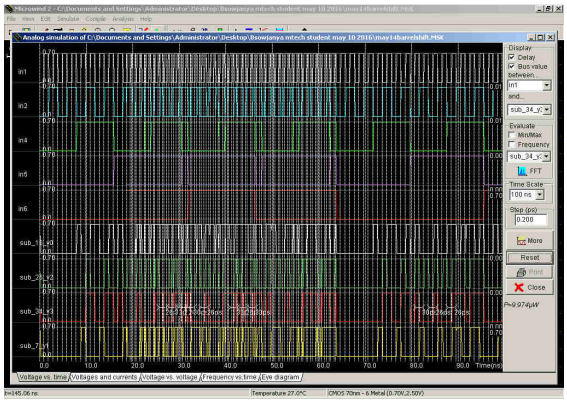

Fig.27:70nm technology waveforms

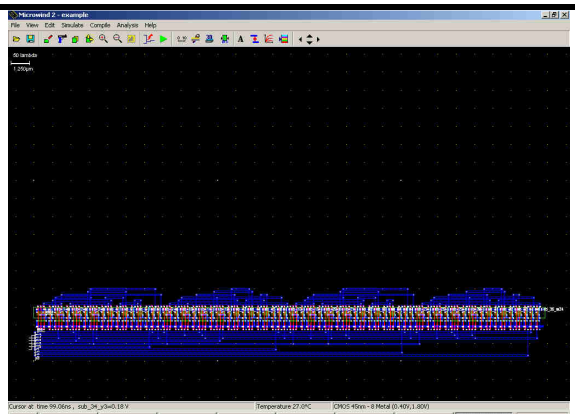

Fig.28: Layout 45 nm

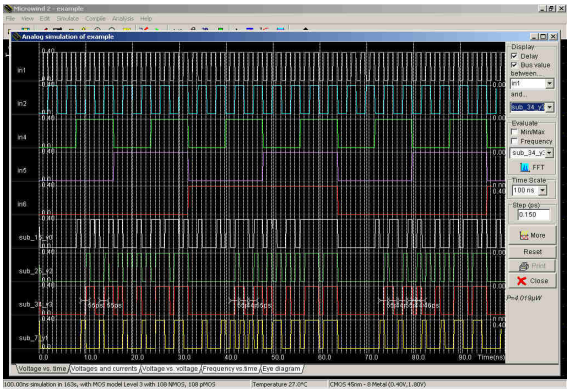

Fig.29: 45nm technology waveforms

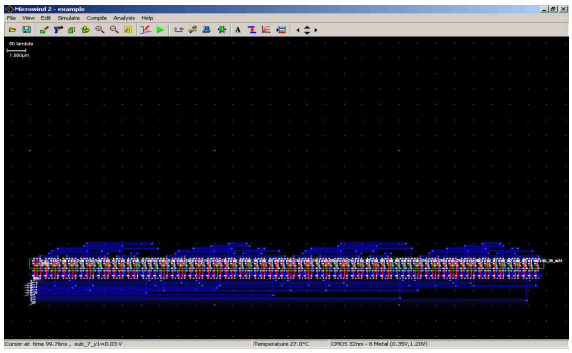

Fig.30:Layout 32 nm

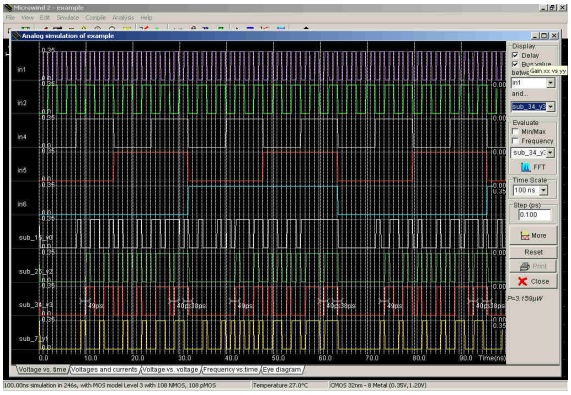

Fig.31:32nm technology waveforms

Table 2: Results

SL. NO	FOUNDRY TECHNOLOGY(nm)	VOLTAGE(volts)	POWER DISSIPATION(µW)
1	250	2.5-2.30	57.10
2	120	1.20-2.5	36.151
3	70	0.7-2.5	9.974
4	45	0.4-1.8	4.019
5	32	0.35-1.2	3.159

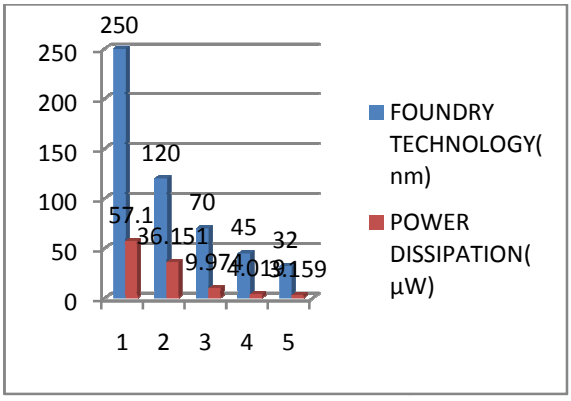

Fig.32: bar graph drawn for different foundry technologies vs power dissipation

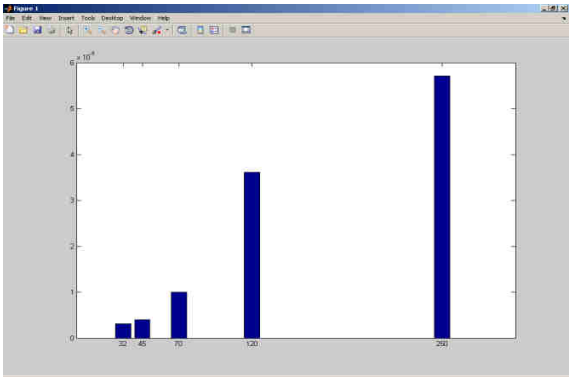

Fig.33: bar graph drawn for different foundry technologies vs power dissipation

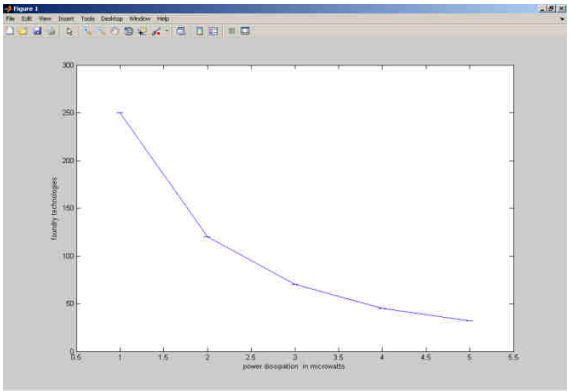

Fig.34: bar graph drawn for different foundry technologies vs power dissipation

III. CONCLUSION

The designed, low power cmos level shifter and barrel shifter circuit have utilized conventional level shifter and 4x1 barrel shifter using MUX used to carry out level-down operations and it is comparably low compared with other designs, hence it is area efficient. This design helps to much reduce power dissipations for multi voltage scaling levels for different foundry technologies**.**

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