https://dx.doi.org/10.22161/ijaers.4.4.24 *ISSN: 2349-6495(P) | 2456-1908(O)*

Implementation & Comparative Analysis of CMOS vs GDI for 8T SRAM Functionality under Power, Delay over Performance

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Abstract— *The Technology behind every electronic gadgets or device has a rapid growth in the market and also in the industry. As all the complex electronic devices are operating at higher frequency and operating in sub threshold region, which leads to delivering higher leakage power at lower operating voltages, and especially when the technology is gradually increasing, mostly in cmos design. So there ought to be a reliable mode of circuit or structure which can be a tradeoff between speed, power and area. So the broad side of this work designates the analysis of Gate diffused input method (GDI) which can be an alternative logic for the implementation of SRAM bit cell instead of CMOS, and relative, comparative analysis of delay & power of CMOS with GDI at 0.4v at 32nm Synopsys tools by obtaining the proper characteristics of ac and dc analysis.*

Keywords— **cmos,** ***GDI, Subthreshold operation, Static, Dynamic power.***

I. INTRODUCTION

The demand for portable electronic devices increasing day by day, as the Technology has a rapid growth in the in industry. As Most of the electronics gadgets are battery operated and increasing the demand for portable and popularity of electronic products, the researchers have driven strive to achieve higher speed and longer battery life.

There were number of techniques proposed in past decades, to reduce the power and leakage, by operating the device under sub threshold region. But generously there are drastic changes in higher leakage power & current. More predominantly this leakage power is dominating the dynamic and static power.

But the problem in the Cmos design is leakage power when the technology is moving on to higher levels. According to the survey given by Intel, leakage power is dominating when the technology is upgrading, as technology has a rapid growth, the amount of complexity of electronic circuits is also increasing according to the customer needs and the relationship is as showed below Fig 1. So there fore, there must be alternating circuit model to reduce the amount of leakage power when the technology has a rapid growth[4].

Cmos circuits plays a vital role in the designing of memory circuit modeling, as it deals with higher switching speed, a basic circuit to implement all the kind of design. an implementation of SRAM is done with 8T model. RAM is one of the main functional unit and takes maximum power especially when it is under dynamic mode of operation The amount of static power is maximum when the circuit is in cutoff state.

This leakage power is dominating the dynamic power when the technology is rapidly growing. SRAM is one of the hearts of the processing element and processing read and writes operations simultaneously. For achieving high performance and more reliable operation, there by changing the different parameters. Therefore the energy consumption per bit is drastically reduced, which will leads to more efficient design. In order to reduce the power consumption of SRAM ,there is relay on different types of process variations like sensing unit, supply voltage, size reduction.

This paper characterizes SRM is design model staring of inverter, 8T SRAM In cmos & GDI of different parameters static and dynamic power, rise and fall time delay & its characteristics by considering the advantages[3][4]

This Paper designated as follows section I clarify operation of cmos inverter, and its characteristics. Section II enlightens the operation GDI inverter. Performance & Implementation of Gate diffused input (GDI) sram in section III. In section IV explains the power analysis of 8T CMOS SRAM. power analysis of GDI 8T SRAM describes in section V. delay estimation of sram cmos is done in section VI.in section VII GDI delay estimation ids done.[1]

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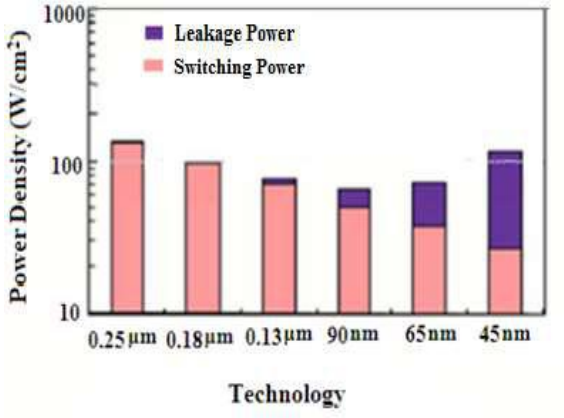

Fig.1: Technology Vs power relationship

Fig.2: power Vs year correlation

II. OPERATION OF CMOS INVERTER

A basic component for the operating of kind logic of sop or pos.The challenges of sub threshold memory design are compromised with inverter operation and shows the circuit diagram of static CMOS inverter circuit. Its operation is readily understood with the simple switch model of the MOS transistor, introducing in the transistor is nothing more than a switch with an infinite off mode resistance for |VGS| < |VT|, and a finite on-resistance for |VGS| > |VT|.

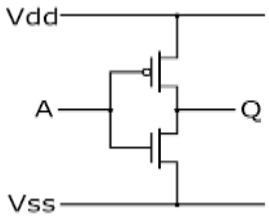

Fig.3: cmos inverter inverter

Performance of the following operation. When input Vin is high and equal to VDD, the NMOS transistor is on state , while the PMOS is off condition . The equivalent circuit of exists between Vout and the ground node, resulting in a steady-state value of 0 V. On the other hand, when the input voltage is low (0 V), NMOS and PMOS transistors are off and on, respectively. And as showed in fig 2.

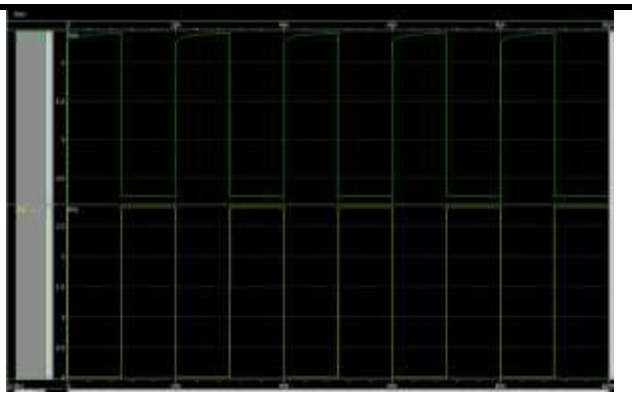

Fig.4 : characteristics of cmos inverter

As the transistor is Low power means operating the design at less than the threshold voltage or sub threshold without degrading the performance. Sub-threshold is one of the methods to achieve low power design. There are basically three Inversion regions:a)Strong inversion region ($V_{gs}>V_t$), b)Moderate inversion region ($V_{gs}=V_t$),c)Weak inversion region ($0 < V_{gs} < V_t$) operation.[2]

The amount of leakage power and delay need to minimize, as the complexity of the circuit is increasing with respect to the technology .and also delay and power is minimized by considering VDD and VSS are also another inputs along with the input.

III. OPERATIONAL ANALYSIS OF GDI CIRCUITS

Gate Diffused Input (GDI) is one of the method and a new technique of digital low power circuit design is operation explained. It allows to reduction of power consumption, delay and area of digital logic circuits, by maintaining lower complexity of logic model design. Performance comparison of traditional CMOS and GDI were presented[3], to reduce layout area, number of logic cells or devices and also to estimate the delay and power, performance is as showed below.whre the gdi has the low swing operation.

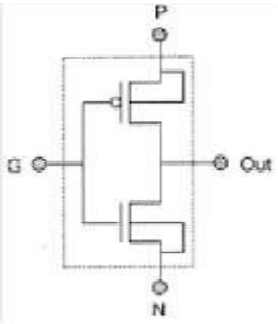

Fig.5: GDI Inverter

The schematic diagram of GDI cell is showed below and the input is applied as a train of pulse with the logic levels are 1 and 0.and another two inputs of vdd and vss are applied as DC signal.

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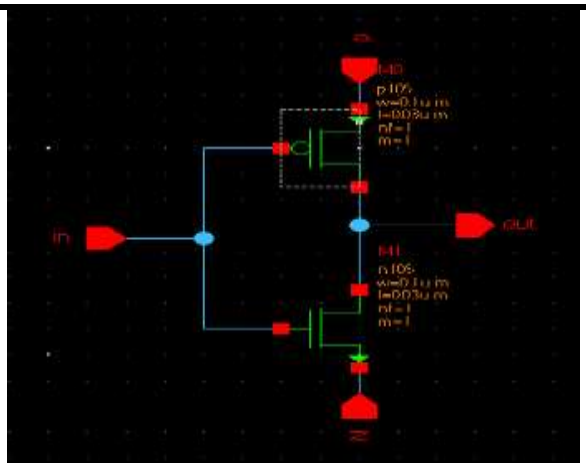

Fig.6: schematic diagram of GDI Inverter

The characteristics of the GDI inverter is as mentioned below. Most of functions are complex in CMOS, as well as in standard logic PTL implementations, but simple as only 2 transistors / function) in GDI design method.[1]

A	B	Functionality	F1
0	0	*pMOSTrans Gate*	V_{Tp}
0	V_{DD}	*CMOSInverter*	V_{DD}
V_{DD}	0	*nMOS Trans Gate*	0
V_{DD}	V_{DD}	*CMOSInverter*	0

Fig.7: Functional characteristics of GDI pass transistor logic

As GDI cell structure is different from existing Pass Transistor Logic techniques, it has some important features, allows to Improvements in design complexity, count of transistor, static power dissipation and low logic level swing.

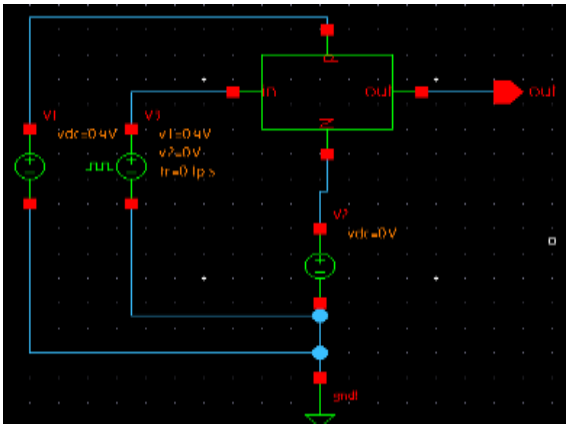

Fig.8: a cell view of representation is done 1 bit

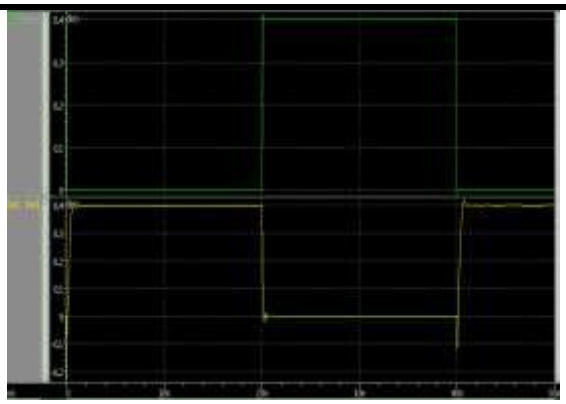

Fig.9: Functional characteristics of GDI inverter logic

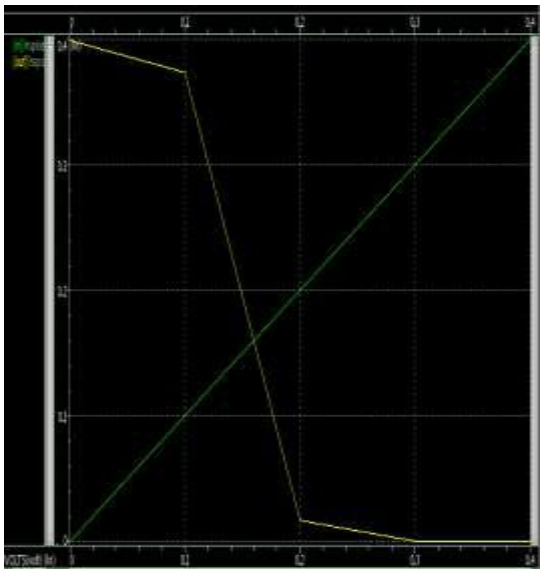

Fig.10: Dc Analysis

An cell view representation is showed in the figure 8 and the dc voltage of 1.5v is applied as input to vdd and vss,and a dc voltage of 0.4v is applied as input to the inverter logic circuit.

IV. GDI BASED 8T SRAM

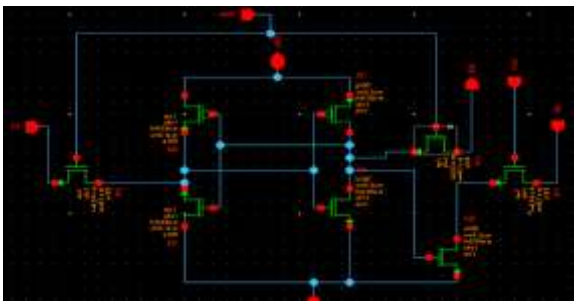

Fig.11: schematic representation of 8T SRAM

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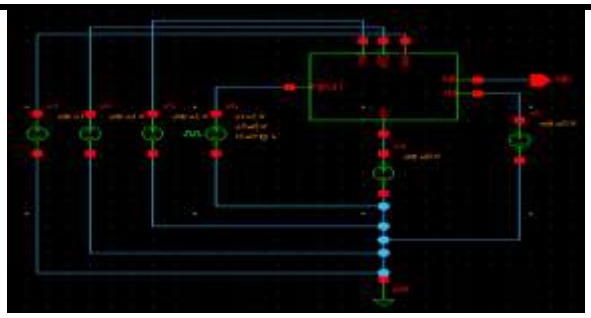

Fig.12: Symbolic view of 8T SRAM

Fig.13: characteristic of 8T GDI SRAM

Power analysis of 8T CMOS SRAM

Static power dissipation

Fig.14: static power Analysis

Static power dissipation= 1.2621 uw

Dynamic power dissipation

Fig.15.Total power dissipation= 7.2593uw

Dynamic Power=Total –Static Power=5.9962 uw

V. POWER ANALYSIS OF 8T GDI SRAM

Static power dissipation

Fig.16: Static power dissipation= 0.668uw

Fig.17: Total power dissipation= 4.073uw

Dynamic Power=Total –Static Power=4.073uw

VI. DELAY ESTIMATION 0F 8T SRAM CMOS

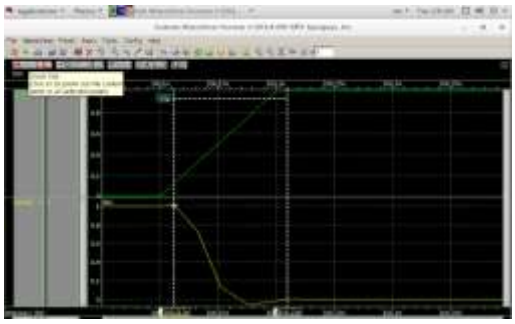

Fig.18: Rise Time Time Delay

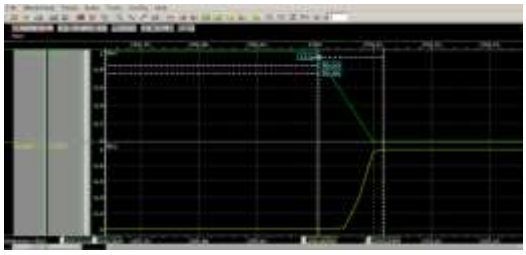

Fig.19 : Fall Time Delay

VII. DELAY ESTIMATION OF 8T SRAM GDI MODEL

Fig.20: Rise & Fall Time Delay

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Comparative Analysis

The following representation indicates the analysis about the power and delay of 8T SRAM implemented in CMOS and GDI.

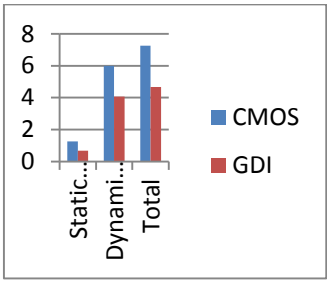
Power analysis micro watts

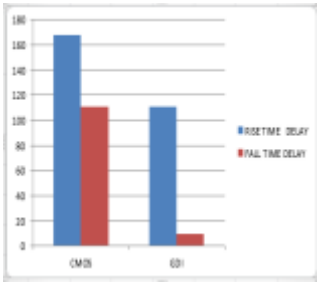
	CMOS	GDI
Static Power	1.2621	0.668
Dynamic Power	5.9962	4.073
Total	7.2583	4.6672

Delay analysis in Pico seconds

Delay in Ps	CMOS	GDI
Rise Time	168	111
Fall Time	111	9.6
Total Delay	279	121

Delay analysis





VIII. CONCLUSION

Static Power is reduced by a factor 63 % dynamic Power is reduced by a factor of 46% and Approximately 55 % on total power but In GDI The Rise Time Is Reduced By 1.5 % And Fall Time Is Decreased By 11%Approximately 6 % on total delay by maintaining the performance.Tolls used were Synopsys Designer -implementation & modelling ,Custom Ic Designer performance and Custom Complier power and delay.

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