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Voltage Scaled Clock Distribution Networks by using low swing D-flip-flop cell

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Abstract—A low-voltage/swing clocking methodology is developed through both circuit and algorithmic innovations. The primary objective is to significantly reduce the power consumed by the clock network while maintaining the circuit performance the same. a novel D-flip-flop (DFF) cell that maximizes power savings by enabling low-voltage/swing operation throughout the entire clock network . In this proposed design of the LSFF is consume the less power compare to existing design. The proposed architecture of this paper is analysis the logic size, area and power consumption using tanner tool.

Index Terms—Clock network, clock tree synthesis (CTS),D-flip-flop (DFF), low power, low-voltage/swing clocking.

I. INTRODUCTION

Power consumption has become one of the primary concerns for almost any application due to increased design complexity, higher integration, and difficulty in scaling the power supply voltage. A clock distribution network consumes 20%–45% of total on-chip power, and 90% of this power is consumed by the flip-flops and last branches of a clock tree. This power dissipation is the result of increased pipelining in an IC, which has led to an increase in the number of flip-flops, and hence the total interconnects length of the clock network. A well-known approach to minimize the overall on-chip power dissipation is to reduce the supply voltage. For example, near-threshold computing has received considerable attention to achieve optimal energy efficiency [6]. A reduction in supply voltage, however, degrades IC performance, particularly when the nominal supply voltages are low [5]. Low-swing (LS) signaling has Fig. 1. Summary of the proposed methodology to achieve LS clocking while maintaining the performance requirements. also been investigated to reduce dynamic power consumed by long interconnects [7]. This approach has been extended to clock networks due to high clock net capacitance.

Clock networks operating at near-threshold voltages have also been investigated. The existing works on LS/voltage clock networks, however, are primarily effective for low-power applications that do not demand high performance. Achieving a reliable LS clock network without sacrificing performance is challenging due to the following issues: 1) clock buffers operating at a lower voltage increase the insertion delay along the clock path, causing higher clock skew; 2) the drive ability of the clock buffers is degraded, producing higher clock slew; and 3) the interface between an LS clock signal and a flip-flop may increase clock-to-Q delay, thereby reducing the timing slack within the data paths while also increasing power consumption.To alleviate the first two issues, a larger number of clock buffers are required, which sacrifice the power savings.To alleviate the third issue, a common approach is to restore full-swing (FS) operation before the clock signal reaches flip-flops [8], [9]. This approach significantly reduces power savings, since the last stage of a clock network has high switching capacitance.In this paper, these three primary issues are simultaneously addressed through both circuit and algorithmic innovations,making LS clocking a practical power reduction strategy for both low-power and high-performance applications. Furthermore, the proposed methodology is implemented within a standard design flow for feasible integration into the existing automation tools. As shown in Fig. 1, the methodology consists of a novel D-flip-flop (DFF) cell and a novel clock tree synthesis (CTS) methodology. The proposed DFF cell enables reliable LS operation at the clock sinks while maintaining the timing constraints the same. The proposed CTS algorithm ensures that the same skew and slew constraints as in FS operation are satisfied. In particular, the proposed methodology has the following characteristics. 1) The proposed LSDFF cell achieves similar clock-to-Q delay as traditional FSDFF topology while consuming less power. Reliable operation is ensured despite an LS clock signal and an FS data signal. 2) The proposed slew-aware LS CTS methodology considers not only capacitance, but also resistance to efficiently utilize clock tree resources at different performance constraints and transistor/interconnect technologies. 3) The increase in the insertion delay due to LS operation on the clock tree is methodically compensated by embedding a buffer insertion/wire snaking scheme within the

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CTS for skew minimization. The output of the proposed methodology is an LS clock tree, running at the same frequency, satisfying the same clock skew and clock slew constraints as the conventional FS operation while saving significant power.

II. EXISTING SYSTEM

A conventional DFF cell designed for FS operation cannot be used when the clock voltage swing is reduced due to degradations in reliability and power consumption.

Reliability: In a typical DFF cell, clock signals drive both nMOS and pMOS transistors. If the same DFF topology is used with an LS clock signal (where as the data signal is still at FS to maintain performance), the pMOS transistors driven by the clock signal fail to completely turn OFF when the clock signal is high. For example, consider a 45-nm technology with a nominal VDD of 1 V. If the clock swing is reduced to 0.7×VDD, the gate-to-source voltage of the pMOS transistors is −0.3 V, since the data signal is at FS and the inverters within the flip-flop are connected to nominal (FS) VDD. Since−0.3 V is sufficiently close to the threshold voltage of pMOS transistors in this technology, this behavior significantly affects the operation reliability of a traditional DFF cell driven by an LS clock signal.

For better illustrate the unreliability of the conventional DFF cells operating with an LS clock signal, a traditional transmission gate-based DFF, as shown in Fig. 1, is simulated with a 45-nm technology node when the clock swing is 0.7 V. Note that the clock signal and the inverted clock signal are internally generated using two inverters. This circuit is referred to as the clock sub circuit, as also shown in Fig. 4. Note that the inverters within the clock sub circuit are connected to a low supply voltage to provide LS clock signals. Since the pMOS transistors driven by the clock signals are not completely turned OFF, internal nodes experience a glitch as high as 400 mV. Furthermore, at the slow corner, the DFF cell fails to correctly latch the data signal. Thus, a new topology is required that can reliably operate with an LS clock signal and an FS data signal.

Power Consumption:

In this case, these inverters also function as single voltage, low-to-high level shifters, and the transmission gates receive FS clock signals. The primary limitation of this approach is an unavoidable increase in power consumption due to significant static current drawn by the inverters within the clock sub circuit. To better illustrate this behavior, a conventional DFF is simulated when an LS clock signal is applied to the clock pin while the clock sub circuit is connected to a nominal VDD.

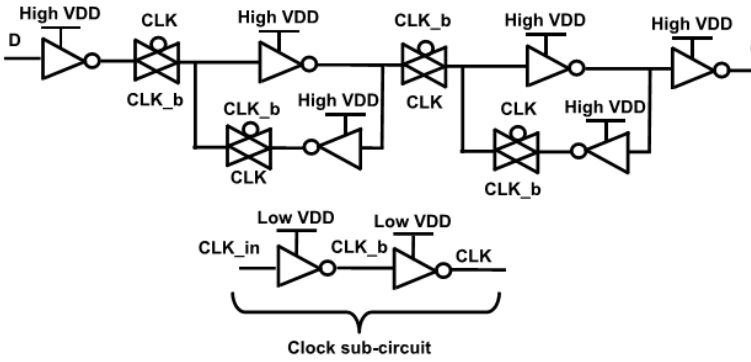

Figure 1: Typical transmission gate-based DFF topology driven by an LS clock

Disadvantages:

- Power consumption is high

III. PROPOSED SYSTEM

The proposed LSDFF cell enables LS operations are performed with the low power consumption level.

1.1.1 Low-Swing D-Flip-Flop Cell:

The proposed DFF topology, shown in Fig. 2, is based on the most commonly used static DFF shown in Fig. 4. Rather than using transmission gates, however, pass gates with nMOS transistors (N1, N2, N5, and N6) are utilized as the switches in both master and slave latches. Thus, when the LS clock signal is at logic high, N1 and N6 can completely turn OFF. Pass gates, however, cannot transfer a full voltage to the output. This issue is critical, since the incoming data signal operates at FS. Thus, node A cannot reach a full VDD, thereby increasing the short circuit and leakage current in the following stages in addition to increasing the clock-to-Q delay. Furthermore, pass transistors are less robust to process variations. To alleviate these issues, a pull-up network consisting of two pMOS transistors are added to both master and slave latches (P1–P4). When the master node M transitions to logic low, P1 turns ON. If the data signal is also at logic low, then node A is pulled to full VDD through P1 and P2. Note that P2 (in the master latch) and P4 (in the slave latch) are added to prevent contention current (and, therefore, reduce power consumption) when the data signal is at logic high and the clock signal is at logic low. In this situation, N1 is ON and node A is discharged through N1 and the inverter. If P2 did not exist, a race condition would occur at node A, since N1 should be stronger than P1, which pulls node Y to full VDD. Finally, pull-down logic (N3, N4, N7, and N8) is added to both master and slave latches to enhance the clock-to-Q delay. In particular, when data and clock signals are at logic low, the pull-down logic is active and pulls master node M to ground, triggering P1. Thus, node A quickly reaches full VDD. Note that the master node does not need to wait for node A to rise through a weak pass

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transistor and activate the inverter. Instead, the pull-down logic completes this transition relatively faster. Also note that the clock sub circuit (not shown in Fig. 1) is identical to the circuit shown in Fig. 1.

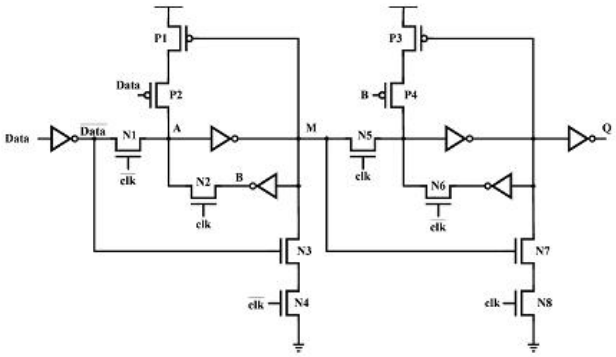

Figure 2: Proposed DFF topology that can reliably work with an LS clock signal whereas the data and output signals are at FS in Transistor level representation.

Advantages:

1. Reduce the power level

Software implementation:

- Tanner EDA

IV. SIMULATION RESULTS

S edits output

Overall architecture

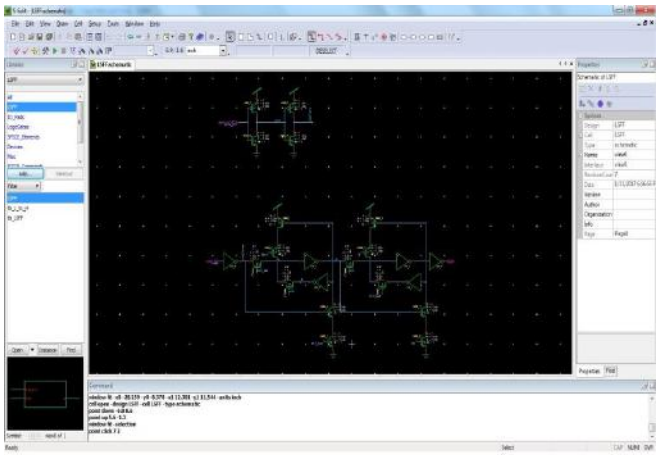

Figure 3: Overall architecture

2. W-edit output

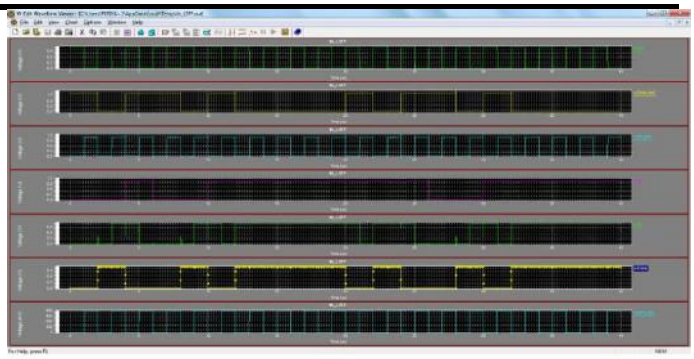

Figure 4: For 45nm

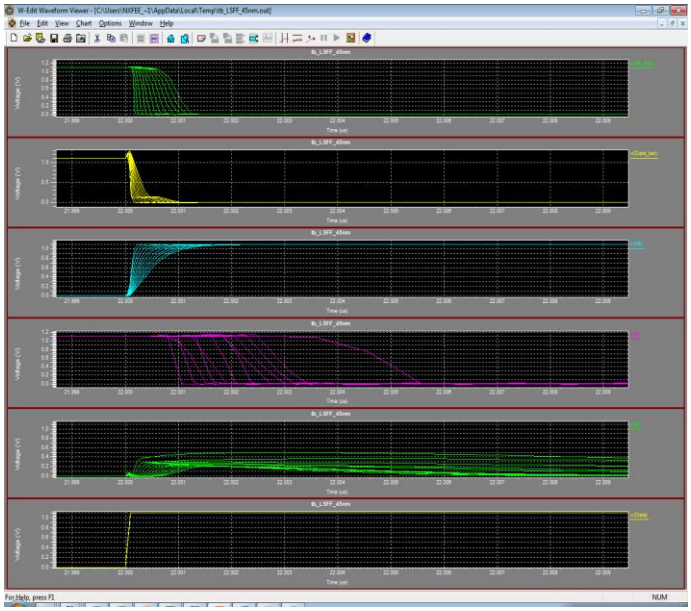

Figure 5: for 45nm with different temperature

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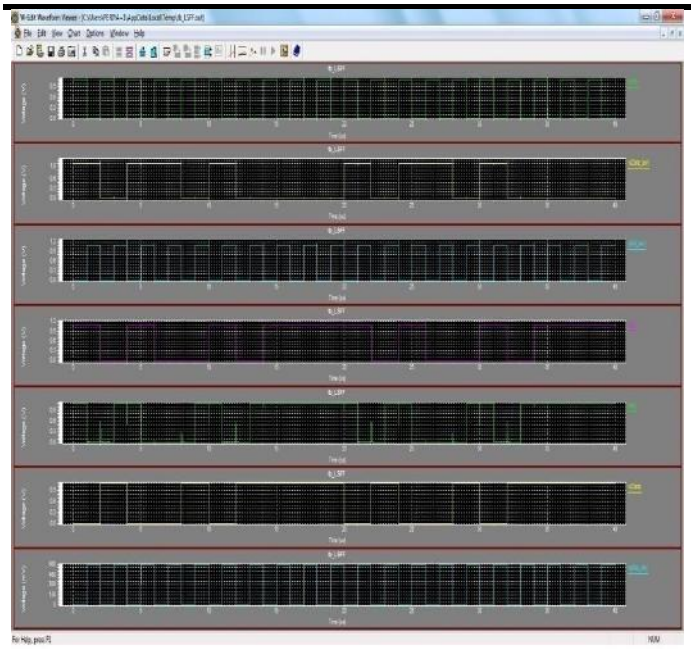

Figure 6: For 32nm

3. Power result

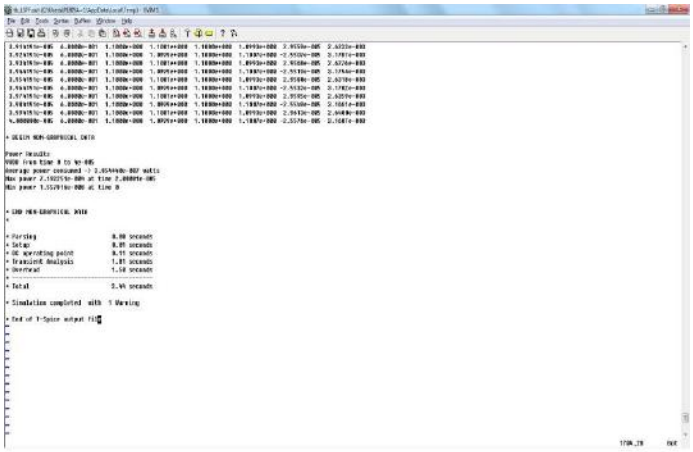

Figure 7: For 45 nm

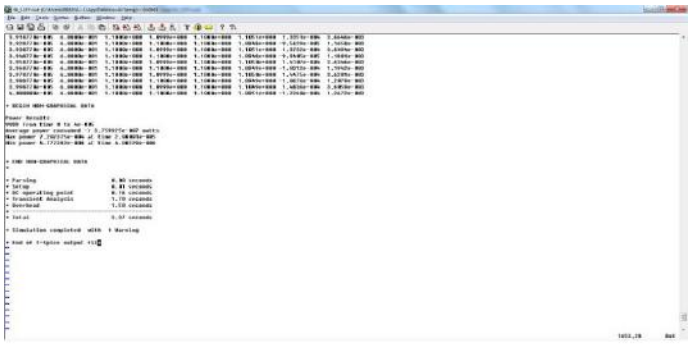

Figure 8: For 32 nm

V. CONCLUSION

A design methodology is proposed for voltage-scaled clock networks operating at a reduced swing. The primary objective is to achieve significant reduction in power consumption without degrading circuit performance. The proposed methodology consists of a novel LSDFF cell. The proposed DFF cell can reliably operate with an LS clock signal, thereby enabling LS operation throughout the entire clock network. Thus, power savings are maximized.

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