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Design & Analysis of an Integrated Dynamic Voltage Restorer-Ultra capacitor with ANFIS Controller for Improving the Power Quality

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Abstract: Quality of the yield control conveyed from the utilities has turned into a noteworthy worry of the advanced ventures for the most recent decade. This power quality related issues are voltage hang, surge, glimmer, voltage irregularity, interferences and symphonious issues. To conquer the issues caused by client side variations from the norm purported custom power gadgets are associated nearer to the heap end. One such dependable client control gadget used to address the voltage droop, swell issue is the Dynamic Voltage Restorer (DVR). It is an arrangement associated custom power gadget, which is thought to be a financially savvy elective when contrasted and other monetarily accessible voltage hang remuneration gadgets. With the combination of ultra- capacitors (UCAP) with the DVR and ANFIS Controller, the UCAP-DVR framework will have dynamic power ability and will have the capacity to freely repay impermanent voltage hangs and swells without depending on the network The proposed framework helps in giving a firm dc-interface voltage, and the coordinated UCAP-DVR-ANFIS framework helps in remunerating transitory voltage droops and voltage swells. The MATLAB/SIMULINK control framework tool stash has been utilized to build up the proposed framework.

Record Terms—DC–DC converter, d–q control, DSP, dynamic voltage restorer (DVR),ANFIS Controller , vitality stockpiling joining, stage bolted circle (PLL), droop/swell, Ultra capacitor (UCAP).

I INTRODUCTION

The electric power framework is thought to be made out of three utilitarian squares - era, transmission and conveyance. For a solid power framework, the era unit must create sufficient energy to take care of client's demand, transmission frameworks must transport mass control over long separations without over-burdening or imperiling framework strength and appropriation frameworks must convey electric energy to every client's premises from mass power frameworks. Dissemination framework finds the finish of energy framework and is associated with the client straightforwardly, so the power quality for the most part relies upon dispersion framework. The purpose for this is the electrical dispersion organizes disappointments represent around 90% of the normal client interferences. In the prior days, the significant concentration for control framework unwavering quality was on era and transmission just as these more capital cost is included in these. Likewise their inadequacy can cause far reaching disastrous outcomes for both society and its condition. In any case, now a day's circulation frameworks have started to get more consideration for unwavering quality evaluation.

At first for the change of energy quality or dependability of the framework FACTS gadgets like static synchronous compensator (STATCOM), static synchronous arrangement compensator (SSSC), interline control stream controller (IPFC), and brought together power stream controller (UPFC) and so forth are presented. These FACTS gadgets are intended for the transmission framework. In any case, now a day's more consideration is on the dispersion framework for the change of energy quality, these gadgets are adjusted and known as custom power gadgets. The fundamental custom power gadgets which are utilized as a part of dispersion framework for control quality change are dissemination static synchronous compensator (DSTATCOM), dynamic voltage Restorer (DVR), dynamic channel (AF), bound together power quality conditioner (UPQC) and so forth.

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In this proposal work from the above custom power gadgets, DVR is utilized with PI controller for the power quality change in the circulation framework. Here two distinct burdens are viewed as, one is direct load and the other is enlistment engine. Diverse blame conditions are considered with these heaps to examine the operation of DVR to enhance the power quality in dissemination framework.

II. THREE PHASE SERIES INVERTER

A. Power Stage

The one-line chart of the framework is appeared in Fig. 1. The power organize is a three-stage voltage source inverter, which is associated in arrangement to the matrix and is in charge of remunerating the voltage lists and swells; the model of the arrangement DVR and its controller is appeared in Fig. 2. The inverter framework comprises of a protected door bipolar transistor (IGBT) module, its entryway driver, LC channel, and a seclusion transformer. The dc-connect voltage Vdc is managed at 260 V for ideal execution of the converter and the line–line voltage Vab is 208 V; in light of these, the tweak file m of the inverter is given by

$$m = \frac{2\sqrt{2}}{\sqrt{3}V_{\mathrm{dc}} * n} V_{ab(\mathrm{rms})}. \qquad (1)$$

Where n is the turn's proportion of the confinement transformer. Substituting n as 2.5 in (1), the required regulation list is computed as 0.52. Consequently, the yield of the dc–dc converter ought to be controlled at 260 V for giving precise voltage remuneration. The goal of the coordinated UCAPDVR framework with dynamic power ability is to make up for impermanent voltage hang (0.1–0.9 p.u.) and voltage swell (1.1–1.2 p.u.), which last from 3 s to 1 min [15].

B. Controller Implementation

There are different techniques to control the arrangement inverter to give dynamic voltage reclamation and the vast majority of them depend on infusing a voltage in quadrature with cutting edge stage, so responsive power is used in voltage rebuilding [3]. Stage propelled voltage reclamation systems are intricate in execution, however the essential explanation behind utilizing these strategies is to limit the dynamic power bolster and in this manner the measure of vitality stockpiling prerequisite at the dc-interface keeping in mind the end goal to limit the cost of vitality stockpiling. In any case, the cost of vitality stockpiling has been declining and with the accessibility of dynamic power bolster at the dc-connect, entangled stage propelled methods can be stayed away from and voltages can be infused in-stage with the framework voltage amid voltage hang or a swell occasion. The control technique requires the utilization of a PLL to discover the turning edge. As examined already, the objective of this venture is to utilize the dynamic power ability of the UCAP-DVR framework and remunerate brief voltage lists and swells.

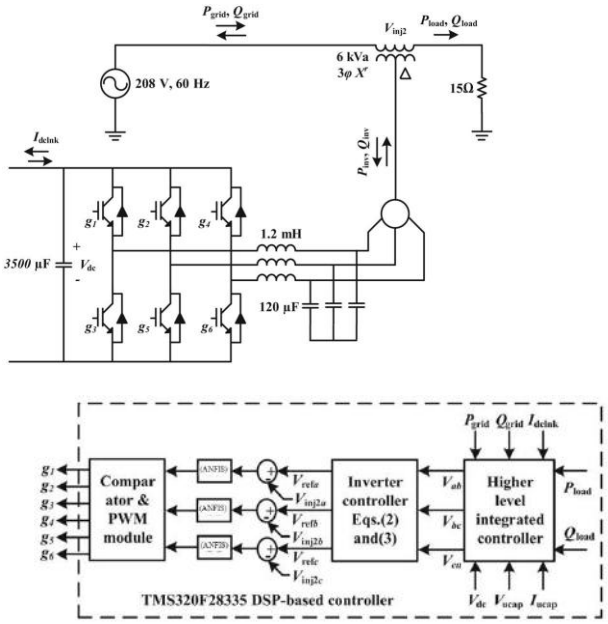

Fig. 2. Model of three-phase series inverter (DVR) and its controller with integrated higher order controller.

The inverter controller usage depends on infusing voltages in-stage with the supply-side line–neutral voltages. This requires PLL for evaluating θ, which has been actualized utilizing the invented control strategy portrayed in [18].

In light of the evaluated θ and the line–line source voltages, Vab, Vbc, and Vca (which are accessible for this delta-sourced framework) are changed into the d–q space and the line– nonpartisan parts of the source voltage Vsa, Vsb, and Vsc, which are not accessible, would then be able to be assessed utilizing

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$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{-1}{2} & \frac{\sqrt{3}}{2} \\ \frac{-1}{2} & \frac{-\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} \cos\left(\theta - \frac{\pi}{6}\right) & \sin\left(\theta - \frac{\pi}{6}\right) \\ -\sin\left(\theta - \frac{\pi}{6}\right) & \cos\left(\theta - \frac{\pi}{6}\right) \end{bmatrix} \begin{bmatrix} \frac{V_d}{\sqrt{3}} \\ \frac{V_q}{\sqrt{3}} \end{bmatrix} \quad (2)$$

$$\begin{bmatrix} V_{\text{ref}a} \\ V_{\text{ref}b} \\ V_{\text{ref}c} \end{bmatrix} = m* \begin{bmatrix} \left(\sin\theta - \frac{V_{sa}}{169.7}\right) \\ \left(\sin\left(\theta - \frac{2\pi}{3}\right) - \frac{V_{sb}}{169.7}\right) \\ \left(\sin\left(\theta + \frac{2\pi}{3}\right) - \frac{V_{sc}}{169.7}\right) \end{bmatrix} \quad (3)$$

$$P_{\text{inv}} = 3V_{\text{inj}2a(\text{rms})} I_{La(\text{rms})} \cos\varphi$$
$$Q_{\text{inv}} = 3V_{\text{inj}2a(\text{rms})} I_{La(\text{rms})} \sin\varphi. \quad (4)$$

III. UCAP AND BIDIRECTIONAL DC–DC CONVERTER WITH ANFIS

A. UCAP Setup

The decision of the quantity of UCAPs essential for giving matrix bolster relies upon the measure of help required, terminal voltage of the UCAP, dc-interface voltage, and dissemination network voltages. In this paper, the exploratory setup comprises of three 48 V, 165F UCAPs (BMOD0165P048) fabricated by Maxwell Technologies, which are associated in arrangement. In this manner, the terminal voltage of the UCAP bank is 144 V and the dc-connect voltage is modified to 260 V. This would give the dc–dc converter a pragmatic working obligation proportion of 0.44–0.72 in the lift mode while the UCAP is releasing and 0.27– 0.55 in the buck mode while the UCAP is charging from the lattice through the dc-connect and the dc–dc converter. It is reasonable and practical to utilize three modules in the UCAP bank.

Accepting that the UCAP bank can be released to half of its underlying voltage (Vuc,ini) to definite voltage (Vuc,fin) from 144 to 72 V, which means profundity of release of 75%, the vitality in the UCAP bank accessible for release is given by

$$E_{\text{UCAP}} = \frac{1}{2} * C * \frac{\left(V_{\text{uc,ini}}{}^2 - V_{\text{uc,fin}}{}^2\right)}{60} W - \text{min}$$
$$E_{\text{UCAP}} = 1/2{*}165/3{*}\left(144^2 - 72^2\right)/60 \quad (5)$$
$$= 7128 \text{ W} - \text{min}.$$

B. Bidirectional DC–DC Converter and Controller

A. UCAP Setup

The decision of the quantity of UCAPs essential for giving matrix bolster relies upon the measure of help required, terminal voltage of the UCAP, dc-interface voltage, and dissemination network voltages. In this paper, the exploratory setup comprises of three 48 V, 165F UCAPs (BMOD0165P048) fabricated by Maxwell Technologies, which are associated in arrangement. In this manner, the terminal voltage of the UCAP bank is 144 V and the dc-connect voltage is modified to 260 V. This would give the dc–dc converter a pragmatic working obligation proportion of 0.44–0.72 in the lift mode while the UCAP is releasing and 0.27– 0.55 in the buck mode while the UCAP is charging from the lattice through the dc-connect and the dc–dc converter. It is reasonable and practical to utilize three modules in the UCAP bank.

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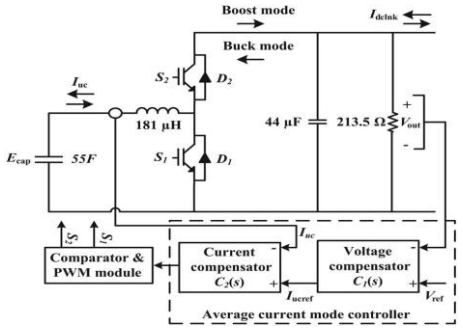

Fig. 3. Model of the bidirectional dc–dc converter and its controller.

A. UCAP Setup

The decision of the quantity of UCAPs vital for giving lattice bolster relies upon the measure of help required, terminal voltage of the UCAP, dc-connect voltage, and circulation network voltages. In this paper, the trial setup comprises of three 48 V, 165F UCAPs (BMOD0165P048) made by Maxwell Technologies, which are associated in arrangement. In this way, the terminal voltage of the UCAP bank is 144 V and the dc-interface voltage is customized to 260 V. This would give the dc–dc converter a pragmatic working obligation proportion of 0.44–0.72 in the lift mode while the UCAP is releasing and 0.27– 0.55 in the buck mode while the UCAP is charging from the matrix through the dc-

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interface and the dc–dc converter. It is functional and financially savvy to utilize three modules in the UCAP bank.

Accepting that the UCAP bank can be released to half of its underlying voltage (Vuc,ini) to definite voltage (Vuc,fin) from 144 to 72 V, which means profundity of release of 75%, the vitality in the UCAP bank accessible for release is given by

$$C_1(s) = 1.67 + \frac{23.81}{s} \quad (6)$$

$$C_2(s) = 3.15 + \frac{1000}{s}. \quad (7)$$

IV DESIGN OF ADAPTIVE NEURO-FUZZY CONTROLLER

Adaptive neuro fuzzy inference system (ANFIS) incorporates the best components of fluffy frameworks and neural systems, and it can possibly catch the advantages of both in a solitary casing work. ANFIS is a sort of manufactured neural system that depends on Takagi-sugeno fluffy derivation framework, which is having one information a done yield. Utilizing a given informational index, the tool kit capacity of ANFIS builds a fluffy deduction framework (FIS) where as the enrollment work parameters are tuned (balanced) utilizing a back spread calculation. Keeping in mind the end goal to have a thought of improved ANFIS engineering for proposed control, an underlying information is produced from typical PI controller and the information is spared in workspace of MATLAB. At that point the ANFIS order window is opened by writing ANFIS proofreader in the primary MATLAB window. At that point the information beforehand spared in workspace is stacked in the ANFIS charge window to create an enhanced ANFIS engineering as appeared in Fig.3.

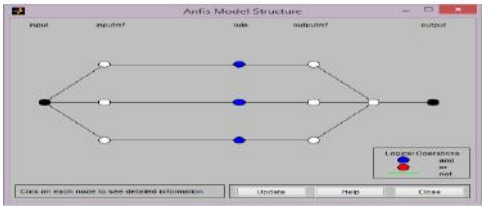

Figure. 4 Optimized ANFIS architecture suggested by MATLAB/ANFIS editor.

In Fig.4 shows schematic of the proposed ANFIS based control architecture. The node functions of each layer in the ANFIS architecture are described as follows:

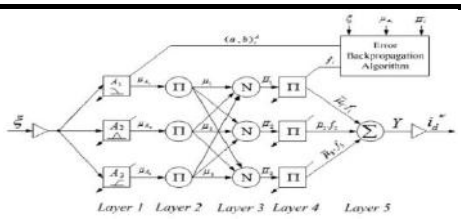

Figure. 5 Schematic of the proposed ANFIS-based control architecture.

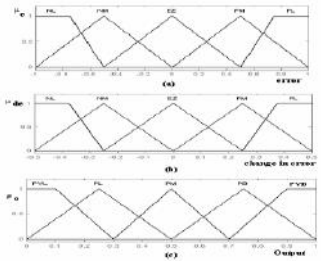

Figure.6 Membership functions for input and output variables for Current Control

de \ e	NL	NM	EZ	PM	PL
NL	PB	PM	PM	PM	PB
NM	PB	PM	PL	PM	PB
EZ	PVB	PM	PVL	PM	PVL
PM	PB	PM	PL	PM	PB
PL	PB	PM	PM	PM	PB

In this work, Sugeno or Takagi-Sugeno-Kang, method of fuzzy inference is used. It is similar to the Mamdani method in many aspects. The first two parts of the fuzzy inference process fuzzifying the inputs and applying the fuzzy operator are exactly the same. The main difference between Mamdani and Sugeno is that the output membership functions of Sugeno are either linear or constant [14] and that of Mamdani output is variable. The procedure involved to develop ANFIS is as follows:

IV SIMULINK MODEL OF THE TEST SYSTEM

The simulation of the proposed UCAP-integrated DVR system is carried out in MATLAB/SIMULINK for a 208 V, 60-Hz system where 208 V is 1 p.u. The system response for a three-phase voltage sag, which lasts for 0.1 s and has a depth of 0.84 p.u., is shown in Fig. 6(a)–(e). It can be observed from Fig. 4(a) that during voltage sag, the source voltage *Vs*rms is reduced to 0.16 p.u. while the load voltage *VL*rms is maintained constant at around 0.9 p.u. due to

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voltages injected *in-phase* by the series inverter.

This can also be observed from the plots of the line–line source voltages [*Vsab*, *Vsbc*, *Vsca*; Fig. 4(b)], the line–line load voltages [*VLab*, *VLbc*, *VLca*; Fig. 6(c)], and the line–neutral injected voltages of the series inverter [*V*inj2*a*, *V*inj2*b*, *V*inj2*c*; Fig. 6(d)]. Finally, it can be observed from Fig. 6(e) that *V*inj2*a* lags *Vsab* by 30◦, which indicates that it is *in-phase* with the line–neutral source voltage *Vsa*. In Fig. 7(a), plots of the bidirectional dc–dc converter are presented and it can be observed that the dc-link voltage *Vf*dc is regulated at 260 V, the average dc-link current *I*dclnkav and the average UCAP current *I*ucav increase to provide the active power required by the load during the sag. Although the UCAP is discharging, the change in the UCAP voltage *E*cap is not visible in this case due to the short duration of the simulation, which is due to limitations in MATLAB/SIMULINK software. It can also be observed from the various active power plots shown in Fig. 7(b) where the power supplied to the load *P*load remains constant even during the voltage sag when the grid power *P*grid is decreasing. The active power deficit of the grid is met by the inverter power *P*inv, which is almost equal to the input power to the inverter *P*dc_*n* available from the UCAP. Therefore, it can be concluded from the plots that the active power deficit between the grid and the load during the voltage sag event is being met by the integrated UCAP-DVR system through the bidirectional dc–dc converter and the inverter. Similar analysis can also be extended for voltage sags, which occur in one of the phases (*a*, *b*, or *c*) or in two of the phases (*ab*, *bc*, or *ca*). However, the active power requirement is greatest for the case where all the three phases ABC experience voltage sag.

The system response for a three-phase voltage swell, which lasts for 0.1 s and has a magnitude of 1.2 p.u., is shown in Fig. 8(a)–(e). It can be observed that during voltage swell, the source voltage *V*srms increases to 1.2 p.u., whereas the load voltage *VL*rms is maintained constant at around 1 p.u. due to voltages injected *in-phase* by the series inverter. This can also be observed from the plots of the line–line source voltages [*Vsab*, *Vsbc*, *Vsca*; Fig. 6(a)], the line–line load voltages [*VLab*, *VLbc*, *VLca*; Fig. 6(b)], and the line–neutral injected voltages of the series inverter [*V*inj2*a*, *V*inj2*b*, *V*inj2*c*; Fig. 8(c)].

Finally, it can be observed that *V*inj2*a* lags *Vsab* by 150◦, which indicates that it is 180◦ out of phase with the line–neutral source voltage *Vsa* as required by the in-phase control algorithm.

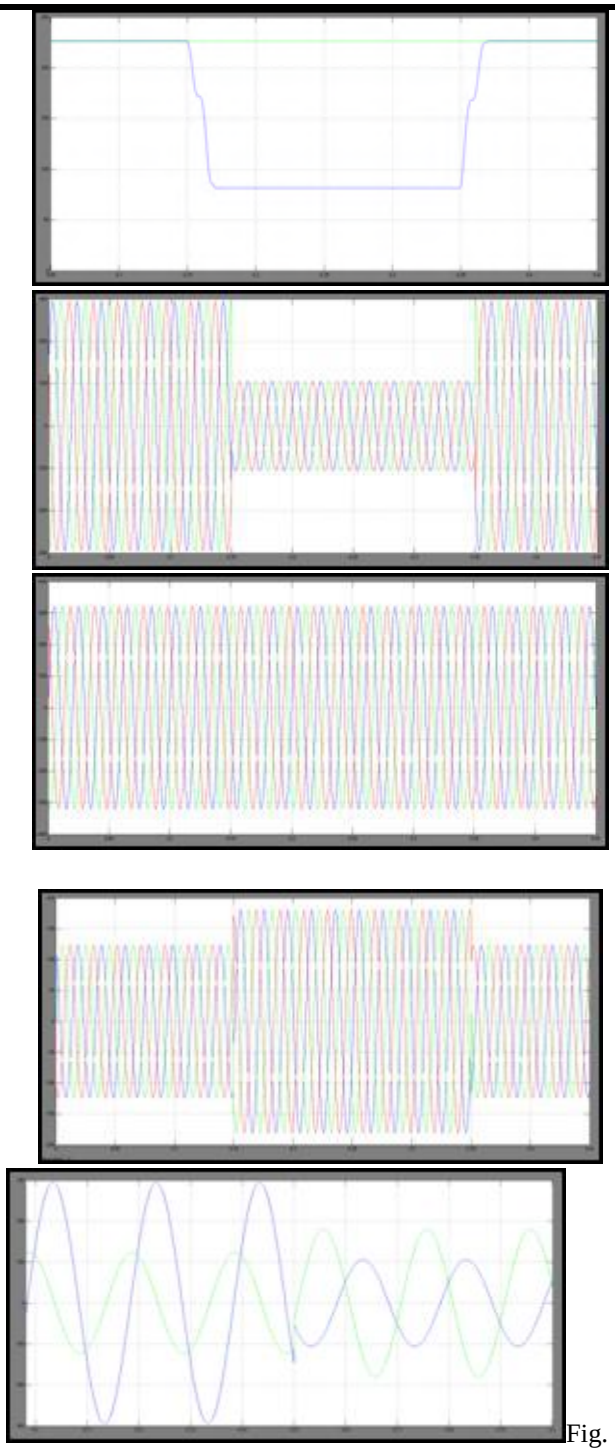

Fig. 7. (a) Source and load RMS voltages *V*srms and *VL*rms during sag.(b) Source voltages *Vsab* (blue), *Vsbc* (red), and *Vsca* (green) during sag.(c) Load voltages *VLab* (blue), *VLbc* (red), and *VLca* (green) during sag.(d) Injected voltages *V*inj2*a* (blue), *V*inj2*b* (red), and *V*inj2*c* (green) during sag.(e) *V*inj2*a* (green) and *Vsab* (blue) waveforms during sag.

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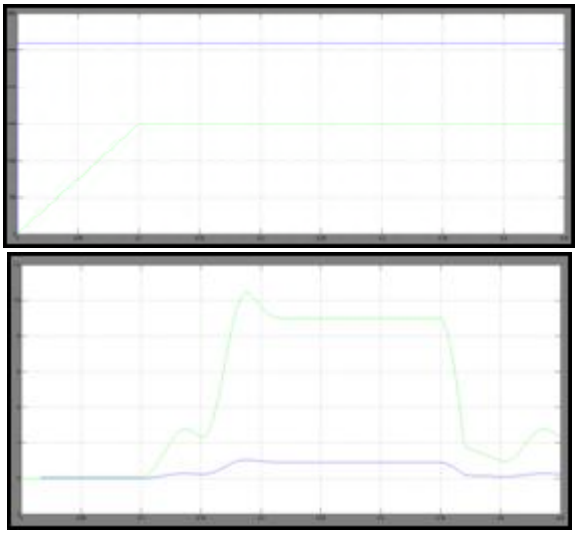
In Fig. 9(a), plots of the bidirectional dc–dc converter are presented and it can be observed that the dc-link voltage *Vf*dc is regulated at 260 V, the average dc-link current *I*dclnkav and the average UCAP current *I*ucav change direction to absorb the additional active power from the grid into the UCAP during the voltage swell event. The overshoot in *I*ucav and *I*dclnkav during startup at 0.1 s and during mode changes at 0.15 and 0.35 s is due to the mismatch between the breaker action and the compensator action in MATLAB/SIMULINK, which is a modeling problem present in the simulation results.

Again, due to MATLAB/SIMULINK limitations, which restrict the duration of the simulation, the increase in *E*cap due to charging of the UCAP during the voltage swell is not visible. This can also be observed from various active power plots where the power supplied to the load *P*load remains constant even during the voltage swell when the grid power *P*grid is increasing.

It can be observed from the inverter power *P*inv and inverter input power *P*dc_in plots that the additional active power from the grid is absorbed by the inverter and transmitted to the UCAP. Therefore, it can be concluded from the plots that the additional active power from the grid during the voltage swell event is being absorbed by the UCAP-DVR system through the bidirectional dc–dc converter and the inverter.



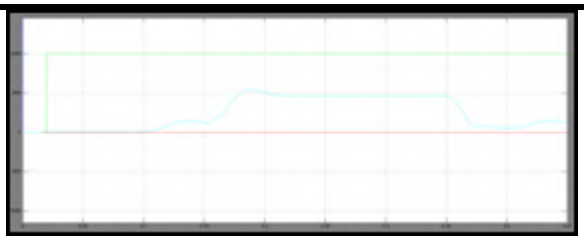


Fig. 8. (a) Currents and voltages of dc–dc converter. (b) Active power of grid, Load, and inverter during voltage sag.

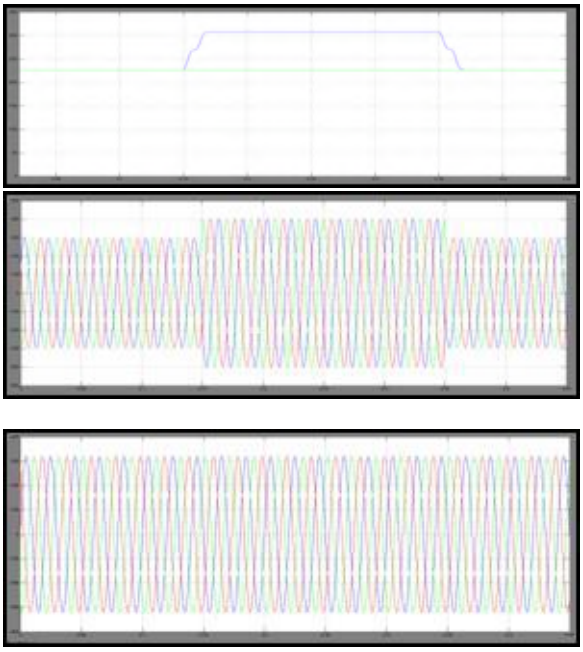
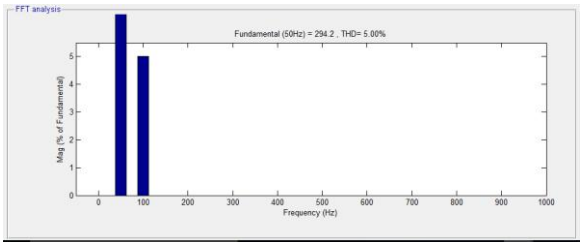


Fig. 9. (a) Source and load rms voltages *Vsrms* and *VLrms* during swell. (b) Source voltages *Vsab* (blue), *Vsbc* (red), and *Vsca* (green) during swell. (c) Load voltages *VLab* (blue), *VLbc* (red), and *VLca* (green) during swell.



(a)

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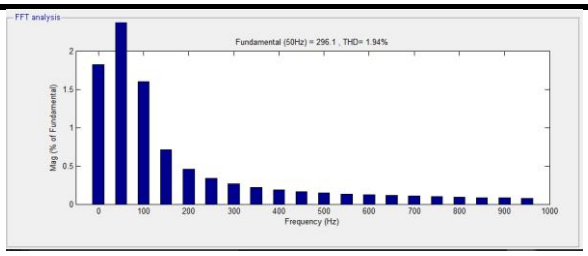

(b)

Fig10. THD variations between conventional Controller & Proposed ANFIS Controller.

Fig 10 shows the THD values comparison between conventional Controller & Proposed ANFIS Controller, It shows the proposed ANFIS controller has 1.94% and conventional controller has 5%.

CONCLUSION

In this work, a fast and cost effective Dynamic Voltage Restorer (DVR) is proposed for mitigating the problem of voltage sag or dip and other fault conditions in industrial distribution systems, specially consisting of the induction motor load. A controller which is based on feed foreword technique is used which utilizes the error signal which is the difference between the reference voltage and actual measured load voltage to trigger the switches of an inverter using a Pulse Width Modulation (PWM) scheme. Here, investigations were carried out for various cases of load at 11kv feeder. It is clear from the results that the power quality of the system with induction motor as load is increased in the sense that the THD and the amount of unbalance in load voltage are decreased with the application of DVR. The effectiveness of DVR using PI controller is established both for linear static load and induction motor load. The simulation of the UCAP-DVR system, which consists of the UCAP, dc–dc converter, and the grid-tied inverter, is carried out using MATLAB/SIMULINK. Hardware experimental setup of the integrated system is presented and the ability to provide temporary voltage sag and swell compensation in all three phases to the distribution grid dynamically is tested. Results for transient response during voltage sags/swells in two phases will be included in the full-version of this paper. Results from simulation and experiment agree well with each other thereby verifying the concepts introduced in this paper. Similar UCAP based energy storages can be deployed in the future on the distribution grid to respond to dynamic changes in the voltage profiles of the grid and prevent sensitive loads from voltage disturbances.

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