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Performance & Analysis of Voltage Controlled DSTATCOM Using External Inductor

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ABSTRACT—*This project proposes theDesign of External Inductor for Improving Performance ofDSTATCOM forbetter Voltage-regulation.A DSTACOM is used for load voltage regulation and its performance mostlyis contingent upon the feeder impedance and its nature (resistive, inductive, stiff, non stiff). On the other hand, a study for investigating voltage regulation performance of DSTATCOM depending upon network parameters is not well defined. This paper aims to provide a comprehensive study of design, operation, and flexible control of a DSTATCOM operating in voltage control mode. A detailed analysis of the voltage regulation capability of DSTATCOM under various feeder impedances is presented. Then, a benchmark design procedure to compute the value of external inductor is presented. A dynamic reference load voltage generation scheme is also developed, which allows DSTATCOM to compensate load reactive power during normal operation, in addition to providing voltage support during disturbances. Simulation and experimental results validate the effective-ness of the proposed scheme.*

Index Terms—*Distribution static compensator (DSTATCOM), power factor, power quality (PQ), voltage control, fuzzy logic controller.*

I. INTRODUCTION

Large electric drives and utility applications require advanced power electronics converter to meet the high power demands. The evolution of power electronic devices, nonlinear loads, and unbalanced loads has degraded the power quality in the power distribution network. The distribution static compensator is a shunt active filter, which injects currents into the point of common coupling (PCC) (the common point where load, source, and DSTATCOM are connected) such that the harmonic filtering, power factor correction, and load balancing can be achieved. In practice, the presence of feeder impedance and nonlinear loads distorts the terminal voltage (PCC) and source currents. The load compensation using state feedback control of DSTATCOM with shunt filter capacitor gives better results. The switching frequency components in the terminal voltages and source currents are eliminated by using state feedback control of shunt filter capacitor. In this situation, DSTATCOM should operate in CCM. However, due to grid faults, source voltage (stiff or non-stiff) can change at any time and then VCM operation is required. DSTATCOM regulates the load voltage by indirectly regulating the voltage across the feeder impedance. When a load is connected to nearly a stiff source, feeder impedance will be negligible. Faults in a widespread power system as well as switching of sizably voluminous loads engender voltage perturbances such as sag and swell in a distribution system [1]. These power quality (PQ) quandaries significantly degrade the performance of sensitive loads like process-control industry, electronics equipment, adjustable drives, etc.

Power quality is one of the most consequential aspects concerned by utility and residential customer, especially when it becomes a very sensitive issue for industrial consumer [1]. Power quality betokens the

faculty to receive pristine electrical voltage sinusoidal waveform at distribution point [1]. It is conspicuous that everyone will aim to gain the excellent quality in every situation no matter in which aspect, and power quality should not be omitted. Power quality quandaries are not incipient issues in a electrical power system and every electrical utilizer might want to minimize their effect on electrical equipment so that the highest possible power quality could be obtained by all of the users [2].

The transmutations of the voltage supplied even for very short period of time, which were not authentically mostly taken attention by public, is now very sumptuous due to their cause of infelicitous operation and shut down situation in manufacturing plants. For the purport of getting the highest

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efficiency in engenderment besides for sustaining of the most plausible operating cost, electrical customers were now agog for the high power quality. For instance, perturbances like voltage sag, which was introduced by the higher fault on the network, will influenced more number of customer victims [1]. Ergo, an opportune study and tenaciousness about the puissance quality perturbances should be conducted solemnly as well as the extenuation manners not only to consummate customers demand, but withal increase the reputation and quality of electrical power in our country.

In order to further understand the sophisticated power quality quandaries, the recordings of all perturbances are now done by installing the on-line power quality monitoring system. Besides that, sundry professional surveys had conducted in date [1]. Hence, it is conspicuously that power quality perturbances are now became the very crucial topic for us to understand and study more. It signifies that the detection and mitigation of voltage sag in electrical power system are withal very paramount to achieve amelioration in power system so that their benefits could be experienced by people in whole country.

From decades to decades, power electronics have been introduced and developed further due to its economical and power preserving advantages. Flexible AC Transmission System (FACTS) are widely used to solve power quality perturbances and Distribution Static Compensator (DSTATCOM) is one of the members of FACTS contrivances family which is efficacious and flexible. Its function is akin to the utilization of synchronous transformer. In other words, DSTATCOM is an expeditious-respond reactive power source compensator, which can opportunely solve varies power perturbances with congruous controller designed, such as voltage sag, voltage swell, flicker, harmonic, and transient. It contains an injection transformer, a voltage source converter (VSC) and a PWM controller with concrete control scheme in order to perform its main function efficient and efficaciously. In this thesis, the function of DSTATCOM in voltage mitigation was mainly be discussed and it is one of the most paramount function of D-STATCOM contrivances.

Conventionally, static var compensator (SVC) is utilized to regulate load voltage, compensate reactive current, and amend transient stability. However, the SVC causes quandaries like harmonic current injection in the system, harmonic amplification, and possible resonance with the source impedance [2]. Distribution static compensator (DSTATCOM) has been proposed to surmount the inhibitions of SVC [3]–[9]. A DSTATCOM is one of the most efficacious solutions to regulate the load voltage. It provides load voltage regulation by supplying fundamental reactive current into source [5], [10]–[15].

However, most of the conventional DSTATCOMs utilized for voltage regulation consider highly inductive and/or significantly astronomically immense feeder impedance [11], [13]. This is conventionally erroneous in a distribution system where feeder impedance used to be resistive in nature [16], [17]. In this scenario, the DSTATCOM will have diminutive voltage regulation capability. Another consequential is-sue is the generation of reference load voltage. In conventional DSTATCOM application for voltage regulation, reference load voltage is set at 1.0 per unit (p.u.) [13]. At this load voltage, voltage-source inverter (VSI) always exchanges reactive power with the source with leading power factor. This causes continuous power losses in the feeder and VSI. Additionally, a conventional DSTATCOM requires high-current rating VSI to provide voltage support [11]. This high-current requisite increases the potency rating of the VSI and engenders more losses in the switches as well as in the feeder.

The voltage regulation performance of DSTATCOM mainly depends upon the feeder impedance and its nature (resistive, inductive, stiff, nonstiff). For voltage control mode (VCM) operation of DSTATCOM and/or grid-connected inverters, the conception of inserting an external inductor in line has been reported [18], [19]. However, in these schemes, only the concept has been introduced leaving ample scope for further investigation and insight into the design details.

The focus of this paper is to provide a detailed design procedure for culling the external inductor which satiates several practical constraints, sanction DSTATCOM to regulate load voltage in stiff as well as resistive feeder, reduce the current requisite for mitigation of sag, and reduce the system losses. With coordinated control of the load fundamental current, terminal voltage, and voltage across the external inductor, a dynamic reference load voltage generation scheme is presented. This scheme ascertains unity power factor (UPF) operation during mundane operation and maintains load voltage constant during voltage perturbances. Detailed simulation and experimental results are included to verify the DSTATCOM performance.

II. DSTATCOM IN THE POWER DISTRIBUTION SYSTEM

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Fig. 1 shows the power circuit diagram of the DSTATCOM topology connected in the distribution system. L_s and R_s are source inductance and resistance, respectively. An external inductance L_{ext} is included in series between load and source points. This inductor helps DSTATCOM to achieve load voltage regulation capability even in worst grid conditions, i.e., resistive or stiff grid. From IEEE-519 standard, point of commoncoupling (PCC) should be the point which is accessible to both the utility and the customer for direct measurement [20]. Therefore, the PCC is the point where *L*ext is connected to the source. The DSTATCOM is connected at the point where load and *L*ext are connected. The DSTATCOM uses a three-phase four-wire VSI. A passive *LC* filter is connected in each phase to filter out high-frequency switching components. Voltages across dc capacitors, *V*dc1 and *V*dc2 , are maintained at a reference value of *V*dcref.

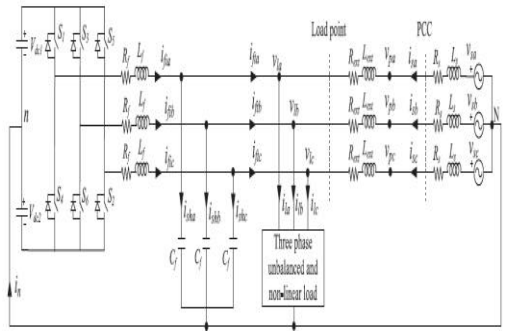

Fig. 1.Three-phase equivalent circuit of DSTATCOM topology in the distribution system.

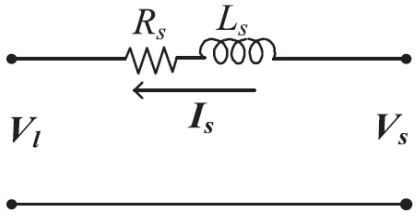

Fig. 2.Equivalent source-load model without considering external inductor.

III. EFFECT OF FEEDER IMPEDANCE ON VOLTAGE REGULATION

To demonstrate the effect of feeder impedance on voltage regulation performance, an equivalent source-load model without considering external inductor is shown in Fig. 2. The current in the circuit is given as

$$\boldsymbol{I}_s = \frac{\boldsymbol{V}_s - \boldsymbol{V}_l}{\boldsymbol{Z}_s} \qquad (1)$$

where $\boldsymbol{V}\,s = Vs\angle\delta$, $\boldsymbol{V}\,l = Vl\angle 0$, $\boldsymbol{I}s = Is\angle\varphi$, and$\boldsymbol{Z}s = Zs\angle\theta s$, with *Vs*, *Vl*, *Is* , *Zs*, δ, φ, and $\theta s$are rms source voltage, rms load voltage, rms source current, feeder impedance, load angle, power factor angle, and feeder impedance angle, respectively. The three-phase average load power (*Pl*) is expressed as

$$P_l = \text{Real}\left[3\,\boldsymbol{V}_l\boldsymbol{I}_s{}^*\right]. \qquad (2)$$

Substituting $\boldsymbol{V}\,l$ and $\boldsymbol{I}s$into (2), the load active power is

$$P_l = \frac{3\,V_l^2}{Z_s}\left[\frac{V_s}{V_l}\cos(\theta_s - \delta) - \cos\,\theta_s\right]. \qquad (3)$$

Rearranging (3), expression for $\delta$is computed as follows:

$$\delta = \theta_s - \cos^{-1}\left[\frac{V_l}{V_s}\left(\cos\,\theta_s + \frac{P_l Z_s}{3\,V_l^2}\right)\right]. \qquad (4)$$

For power transfer from source to load with stable operation in an inductive feeder, δmust be positive and less than 90◦. Also, all the terms of the second part of (4), i.e., inside cos−1, are amplitude and will always be positive. Therefore, the value of the second part will be between "0" and "π/2" for the entire operation of the load. Consequently, the load angle will lie between $\theta s$and ($\theta s - \pi/2$) under any load operation, and therefore, maximum possible load angle is θs. The vector expression for source voltage is given as follows:

$$\boldsymbol{Vs} = Vl + IsZs\angle(\theta s + \varphi). \qquad (5)$$

A DSTATCOM regulates the load voltage by injecting fundamental reactive current. To demonstrate the DSTATCOM voltage regulation capability at different supply voltages for different *Rs/Xs*, vector diagrams using (5) are drawn in Fig. 3. To draw these diagrams, load voltage *Vl*is taken as reference phasor having the nominal value*OA*(1.0 p.u.).With aim of making *Vl*= *Vs*= 1.0 p.u., locus of *Vs*will be a semicircle of radius *Vl*. Since the maximum possible load angle is 90◦ in an inductive feeder, phasor***Vs***can be anywhere inside curve *OACBO*. It can be seen that the value of $\theta s + \varphi$must be greater than 90◦ for zero voltage regulation. Additionally, it is possible only when power factor is leading at the load terminal as θscannot be more than 90◦.

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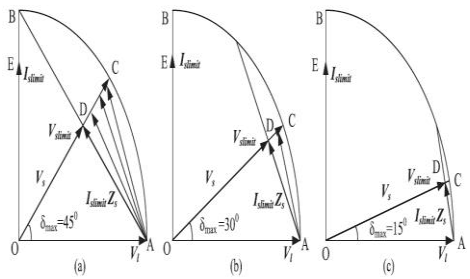

Fig. 3. Voltage regulation performance curve of DSTATCOM at different *Rs/Xs*. (a) For *Rs/Xs*= 1. (b) For *Rs/Xs*=√3. (c) For *Rs/Xs*= 3.73

Fig. 3(a) shows the limiting case when *Rs/Xs*= 1, i.e., *θs*= 45◦. From (4), the maximum possible load angle is 45◦. The maximum value of angle, *θs*+ *φ*, can be 135◦ when *φ*is 90◦. Hence, the limiting source current phasor*OE*, which is denoted by *I*slimit, will lead the load voltage by 90◦. Lines *OC* and *AB* show the limiting vectors of *V*sand *IsZs*, respectively, with*D*as the intersection point. Hence, area under *ACDA* shows the operating region of DSTATCOM for voltage regulation. The point *D* has a limiting value of *V*slimit = *IsZs*= 0.706 p.u. Therefore, maximum possible voltage regulation is 29.4%. However, it is impossible to achieve these two limits simultaneously as *δ*and *φ*cannot be maximum at the same time. Again if *Zs*is low, the source current, which will be almost inductive, will be enough to be realized by the DSTATCOM.

Fig. 3(b) considers case when *Rs/Xs*=√3, i.e., *θs*= 30◦. The area under *ACDA* shrinks, which shows that with the increase in *Rs/Xs* from the limiting value, the voltage regulation capability decreases. In this case, the limiting values of *V*s limit and *IsZs* are found to be 0.866 and 0.5 p.u., respectively. Here, maximum possible voltage regulation is 13.4%.However, due to high-current requirement, a practical DSTATCOM can provide very small voltage regulation.

Voltage regulation performance curves for more resistive grid, i.e., *θs*=15◦, as shown in Fig. 3(c), can be drawn similarly. Here, area under*ACDA*is negligible. For this case, hardly any voltage regulation is possible. Therefore, more the feeder is resistive in nature, lesser will be the voltage regulation capability. Therefore, it is inferred that the voltage regulation capability of DSTATCOM in a distribution system mainly depends upon the feeder impedance. Due to resistive nature of feeder in a distribution system, DSTATCOM voltage regulation capability is limited. Moreover, very high current is required to mitigate small voltage disturbances, which results in higher rating of insulated-gate bipolar transistor switches as well as increased losses. One more point worth to be noted is that, in the resistive feeder, there will be some voltage drop in the line at nominal source voltage which the DSTATCOM may not be able compensate to maintain load voltage at 1.0 p.u. even with an ideal VSI.

IV. SELECTION OF EXTERNAL INDUCTOR FOR VOLTAGE REGULATION IMPROVEMENT AND RATING REDUCTION

This section presents a generalized procedure to select external inductor for improvement in DSTATCOM voltage regulation capability while reducing the current rating of VSI. Fig. 4 shows single-phase equivalent DSTATCOM circuit diagram in distribution system.With balanced voltages, source current will be

$$\boldsymbol{I}_s = \frac{V_s\angle\delta - V_l\angle 0}{(R_s + R_{\text{ext}}) + j\,(X_s + X_{\text{ext}})} = \frac{V_s\angle\delta - V_l\angle 0}{R_{\text{sef}} + jX_{\text{sef}}} \qquad (6)$$

where*R*sef = *Rs*+ *R*ext and *X*sef = *Xs*+ *X*ext are effective feeder resistance and reactance, respectively. *R*ext is equivalent series resistance (ESR) of external inductor, and will be small. With *θ*sef = tan−1 *X*sef*R*sef and *Z*sef = _ *R*2 sef + *X*2 sef as effective impedance angle and effective feeder impedance, respectively, the imaginary component of ***I****s*is given as

$$I_s^{im} = \frac{V_l \sin\theta_{\text{sef}} + V_s \sin(\delta - \theta_{\text{sef}})}{Z_{\text{sef}}}. \qquad (7)$$

With the addition of external impedance, the effective feeder impedance becomes predominantly inductive. Hence, *Z*sef≈ *X*sef. Therefore, approximated *Iim s* will be

$$I_s^{im} = \frac{V_l \sin\theta_{\text{sef}} + V_s \sin(\delta - \theta_{\text{sef}})}{X_{\text{sef}}}. \qquad (8)$$

DSTATCOM Power rating (*Svsi*) is given as follows [21]:

$$S_{\text{vsi}} = \sqrt{3}\,\frac{V_{\text{dc}}}{\sqrt{2}}\,I_{\text{vsi}} \qquad (9)$$

Where *I*vsi is the rms phase current rating of the VSI and *V*dc is the voltage maintained at the dc capacitors. The DSTATCOM aims to inject harmonic and reactive current component of load currents. Suppose *Iim l* is the maximum rms reactive and harmonic current rating of the load; then, the value of compensator current used for voltage regulation (same as *Iims*) is obtained by subtracting *Iim l* from *I*vsi and given as follows:

$$I = I_{\text{vsi}} - I_l^{im} = \frac{\sqrt{2}S_{\text{vsi}}}{\sqrt{3}V_{\text{dc}}} - I_l^{im}. \qquad (10)$$

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Comparing (8) and (10) while using the value of $\delta$from (4), the following expression is obtained:

$$X_{\text{sef}} = \frac{V_l \sin\theta_{\text{sef}} - V_s \sin\left[\cos^{-1}\left[\frac{V_l}{V_s}\left(\cos\theta_{\text{sef}} + \frac{P_l X_{\text{sef}}}{3V_l^2}\right)\right]\right]}{\frac{\sqrt{2}S_{\text{vsi}}}{\sqrt{3}V_{\text{dc}}} - I_l^{lm}}. \quad (11)$$

The above expression is used to compute the value of external inductor. A design example of external inductor, used for this study, is given in the next section.

V. DESIGN EXAMPLE OF EXTERNAL INDUCTOR

Here, it is assumed that the considered DSTATCOM protects load from a voltage sag of 60%. Hence, source voltage V_s=0.6 p.u. is considered as worst case voltage disturbances.During voltage disturbances, the loads should remain operational while improving the DSTATCOM capability to mitigate the sag. Therefore, the load voltage during voltage sag is maintained at 0.9 p.u., which is sufficient for satisfactory operation of the load. In the present case, maximum required value of $I_l^{lm}$is 10 A. With the system parameters given inTable I, theeffective reactance after solving (11) is found to be 2.2 Ω (L_{sef} = 7 mH). Hence, value of external inductance, L_{ext}, will be 6.7 mH.

This external inductor is selected while satisfying the constraints such as maximum load power demand, rating of DSTATCOM, and amount of sag to be mitigated. In this design example, for base voltage and base power rating of 400 V and 10 kVA, respectively, the value of external inductance is 0.13 p.u. Moreover, with a total inductance of 7 mH (external and actual grid inductance), the total impedance will be 0.137 p. u. The short-circuit capacity of the line will be 1/0.13 = 7.7 p.u., which is sufficient for the satisfactory operation of the system. Additionally, a designer always has flexibility to find suitable value of L_{ext} if the constraints are modified or circuit conditions are changed. Moreover, the conventional DSTATCOM operated for achieving voltage regulation uses large feeder inductances [11], [13].

TABLE I

SIMULATION PARAMETERS

System quantities	Values
Source voltage	230 V rms L-N (1.0 p.u.), 50 Hz
Feeder impedance	$R_s = 0.3\ \Omega$, $L_s = 0.3$ mH, $R_s/X_s = 3.185$
External impedance	$L_{\text{ext}} = 6.7$ mH, $R_{\text{ext}} = 0.07\ \Omega$
Linear load	$Z_{la} = 30 + j62.8\ \Omega$, $Z_{lb} = 40 + j78.5\ \Omega$, $Z_{lc} = 50 + j50.24\ \Omega$
Nonlinear load	Three-phase rectifier supplying *RL* load of 50 Ω and 200 mH
VSI parameters	$V_{\text{dc}} = 520$ V, $C_{\text{dc}} = 2600\ \mu$F, $L_f = 5$ mH, $C_f = 20\ \mu$F, $S_{\text{vsi}} = 30$ kVA
PI gains	$K_{p\delta} = 8.5\,e^{-7}$, $K_{i\delta} = 1.8\,e^{-6}$

With the external inductance while neglecting its ESR, R_s /X_{sef}will be 0.13, i.e.,θ_{sef}= 83˚. Voltage regulation performance curves of the DSTATCOM in this case are shown in Fig. 5, of the stable operating range *OABO*. Hence, introduction of external inductor greatly improves the DSTATCOM voltage regulation capability. Additionally, due to increased effective feeder impedance, the current requirement for sag mitigation also reduces. Moreover, if ESR of the external inductor is included, then the equivalent feeder impedance angle changes slightly (i.e., from 83◦ to 80.45◦) and has negligible effect on the expression obtained in (11) as well as the voltage regulation capability of the DSTATCOM.

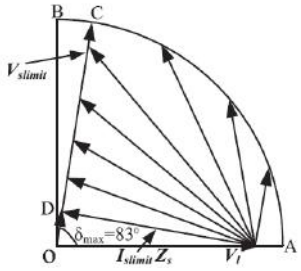

Fig. 5.Voltage regulation performance of DSTATCOM with external inductance.

VI. FUZZY LOGIC CONTROL

L. A. Zadeh presented the first paper on fuzzy set theory in 1965. Since then, a new language was developed to describe the fuzzy properties of reality, which are very difficult and sometime even impossible to be described using conventional methods. Fuzzy set theory has been widely used in the control area with some application to power system [5]. A simple fuzzy logic control is built up by a group of rules based on the human knowledge of system behavior. Matlab/Simulink simulation model is built to study the dynamic behavior of converter. Furthermore, design of fuzzy logic controller can provide desirable both small signal and large signal dynamic performance at same time, which is not

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possible with linear control technique. Thus, fuzzy logic controller has been potential ability to improve the robustness of compensator. The basic scheme of a fuzzy logic controller is shown in Fig.3 and consists of four principal components such as: a fuzzy fication interface, which converts input data into suitable linguistic values; a knowledge base, which consists of a data base with the necessary linguistic definitions and the control rule set; a decision-making logic which, simulating a human decision process, infer the fuzzy control action from the knowledge of the control rules and linguistic variable definitions; a de-fuzzification interface which yields non fuzzy control action from an inferred fuzzy control action [10].

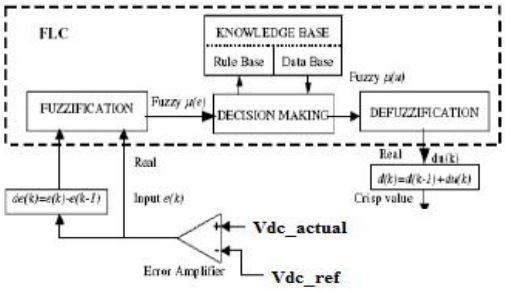

Fig.3. Block diagram of the Fuzzy Logic Controller (FLC).

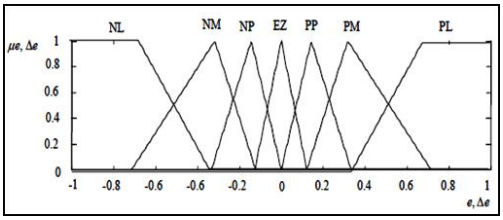

Fig.4 Membership functions for Input, Change in input, Output.

Rule Base: the elements of this rule base table are determined based on the theory that in the transient state, large errors need coarse control, which requires coarse in-put/output variables; in the steady state, small errors need fine control, which requires fine input/output variables. Based on this the elements of the rule table are obtained as shown in Table 1, with „V_{dc}" and$V_{dc\text{-}ref}$ as inputs.

This sections presents a flexible control strategy to improve the performance of DSTATCOM in presence of the external inductor *L*ext. First, a dynamic reference load voltage based on the coordinated control of the load fundamental current, PCC voltage, and voltage across the external inductor is computed. Then, a proportional-integral (PI) controller is used to control the load angle, which helps in regulating the dc bus voltage at a reference value. Finally, three-phase reference load voltages are generated. The block diagram of the control strategy is shown in Fig. 6.

TABLE I:

Δe \ e	NL	NM	NS	EZ	PS	PM	PL
NL	NL	NL	NL	NL	NM	NS	EZ
NM	NL	NL	NL	NM	NS	EZ	PS
NS	NL	NL	NM	NS	EZ	PS	PM
EZ	NL	NM	NS	EZ	PS	PM	PL
PS	NM	NS	EZ	PS	PM	PL	PL
PM	NS	EZ	PS	PM	PL	PL	PL
PL	NL	NM	NS	EZ	PS	PM	PL

A. Derivation of Dynamic Reference Voltage Magnitude (*V*l*)

In conventional VCM operation of DSTATCOM, the reference load voltage is maintained at a constant value of 1.0 p.u. [10]–[12]. Source currents cannot be controlled in this reference generation scheme. Therefore, power factor will not be unity and source exchanges reactive power with the system even at nominal supply. To overcome this limitation, a flexible control strategy is developed to generate reference load voltage. This scheme allows DSTATCOM to set different reference voltages during various operating conditions. The scheme is described in the following.

1) Normal Operation: It is defined as the condition when load voltage lies between 0.9 and 1.1 p.u. In this case, the proposed flexible control strategy controls load voltages such that the source currents are balanced sinusoidal and VSI does not exchange any reactive power with the source. Hence, the source supplies only fundamental positive-sequence current component to support the average loads power and VSI losses. Reference source currents ($i* sj$, where $j = a, b, c$ are three phases), computed using instantaneous symmetrical component theory [22], are given aswhere the area under *AC DA* covers the majority

$$i_{sj}^{*} = \frac{v_{pj1}^{+}}{\Delta_1^{+}}(P_l + P_{\text{loss}}) \qquad (12)$$

where $\Delta^{+}_1 = \Sigma\ j{=}a,b,c(v{+}\ pj1\ )2$. The voltages $v{+}\ pa1$,$v{+}\ pb1$, and $v{+}\ pc1$ are fundamental positive-sequence components of PCC voltages. Average load power (*Pl*) and VSI losses (*P*loss) are calculated using moving average filter (MAF) as follows:

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$$P_l = \frac{1}{T}\int_{t_1-T}^{t_1} (v_{la}i_{la} + v_{lb}i_{lb} + v_{lc}i_{lc})\, dt \qquad (13)$$

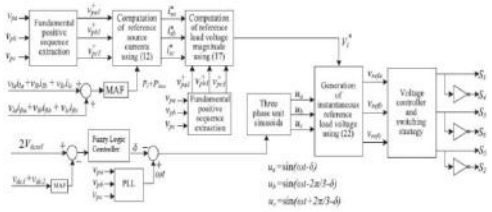

Fig. 6. Block diagram of the proposed flexible control strategy.

$$P_{\text{loss}} = \frac{1}{T}\int_{t_1-T}^{t_1} (v_{la}i_{fta} + v_{lb}i_{ftb} + v_{lc}i_{ftc})\, dt. \qquad (14)$$

The reference source currents must be in phase with the respective fundamental positive-sequence PCC voltages for achieving UPF at the PCC. Instantaneous PCC voltage and reference source current in phase-*a* can be defined as follows:

$$v_{pa1}^{+} = \sqrt{2}V_{pa1}^{+}\sin(\omega t - \varphi_{pa1}^{+}),\ i_{sa}^{*} = \sqrt{2}I_{sa}^{*}\sin(\omega t - \varphi_{pa1}^{+}) \qquad (15)$$

where$V$ + $pa1$ and ϕ+ $pa1$ are rms voltage and angle of fundamental positive-sequence voltage in phase-*a*, respectively. $I^{*}_{sa}$is the rms reference source current obtained from (12). With external impedance, the expected load voltage is given as follows:

$$\boldsymbol{V}_{la} = \boldsymbol{V}_{pa1}^{+} - \boldsymbol{I}_{sa}^{*}\, Z_{\text{ext}}. \qquad (16)$$

From (15) and (16), the load voltage magnitude will be

$$V_{la} = \sqrt{\left[\left(V_{pa1}^{+}\cos\varphi_{pa1}^{+} - I_{sa}^{*}\, Z_{\text{ext}}\cos\left(\theta_{ext} - \varphi_{pa1}^{+}\right)\right)^2 + \left(V_{pa1}^{+}\sin\varphi_{pa1}^{+} - I_{sa}^{*}Z_{\text{ext}}\sin\left(\theta_{ext} - \varphi_{pa1}^{+}\right)\right)^2\right]}. \qquad (17)$$

With UPF at the PCC, the voltage across the external inductor will lead the PCC voltage by 90◦. Neglecting ESR of external inductor, it can be observed that the voltage across external inductor improves the load voltage compared to the PCC voltage.

This highlights another advantage of external inductor where it helps in improving the load voltage. As long as *Vla*lies between 0.9 and 1.1 p.u., same voltage is used as reference terminal voltage ($V * l$), i.e.,

$$\text{if } V_{la} \in [0.9 - 1.1 \text{ p.u.}],\ \text{then } V_l^{*} = V_{la}. \qquad (18)$$

2) Operation During Sag: Voltage sag is considered when value of (18) is less than 0.9 p.u. To keep filter current minimum, the reference voltage is set to 0.9 p.u. Therefore,

$$V_l^{*} = 0.9 \text{ p.u.} \qquad (19)$$

3) Operation During Swell: A voltage swell is considered when any of the PCC phase voltage exceeds 1.1 p.u. In this case, reference load voltage ($V * l$) is set to 1.1 p.u., which results in minimum current injection. Therefore,

$$V_l^{*} = 1.1 \text{ p.u.} \qquad (20)$$

B. Computation of Load Angle (δ)

Average real power at the PCC (Ppcc) is sum of average load power (Pl) and VSI losses (Ploss). The real power Ppcc is taken from the source depending upon the angle between source and load voltages, i.e., load angle δ. If DSTATCOM dc bus capacitor voltage is regulated to a reference value, then in steady-state condition, Ploss is a constant value and forms a fraction of Ppcc. Consequently, $\delta$is also a constant value.

The dc-link voltage is regulated by generating a suitable value of δ. The average voltage across dc capacitors (Vdc1 + Vdc2) is compared with a reference voltage and error is passed through a PI controller. Output of PI controller, δ, is given as

$$\delta = K_{p\delta}\, e_{\text{vdc}} + K_{i\delta}\int e_{\text{vdc}}\, dt \qquad (21)$$

Where vdc = 2Vdcref − (Vdc1 + Vdc2) is the voltage error. $Kp\delta$ and $Ki\delta$ are proportional and integral gains, respectively.

C. Generation of Instantaneous Reference Voltage

Selecting suitable reference load voltage magnitude and computing load angle $\delta$from (21), the three-phase balanced sinusoidal reference load voltages are given as follows:

$$\begin{aligned} v_{refa} &= \sqrt{2}\, V_l^{*}\ \sin(\omega t - \delta) \\ v_{refb} &= \sqrt{2}\, V_l^{*}\ \sin(\omega t - 2\pi/3 - \delta) \\ v_{refc} &= \sqrt{2}\, V_l^{*}\ \sin(\omega t + 2\pi/3 - \delta). \end{aligned} \qquad (22)$$

These voltages are realized by the VSI using a predictive voltage controller [23].

VIII. MATLAB/SIMULINK RESULTS

The control scheme is implemented using PSCAD software. Simulation parameters are given in Table I. Terminal voltages and source currents before compensation

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are plotted in Fig. 7 . Distorted and unbalanced source currents flowing through the feeder make terminal voltages unbalanced and distorted. Three conditions, namely, nominal operation, operation during sag, and operation during load change are compared between the traditional and proposed method. In the traditional method, the reference voltage is 1.0 p.u. [2], [8]–[11], whereas in the proposed method used to find the reference voltage.

A. Nominal Operation

Initially, the traditional method is considered. Fig. 8(a)–(c) shows the regulated terminal voltages and corresponding source currents in phases. These waveforms are balanced and sinusoidal. However, source currents lead respective terminal voltages which show that the compensator supplies reactive current to the source to overcome feeder drop, in addition to supplying load reactive and harmonic currents. Fig. 9(a)

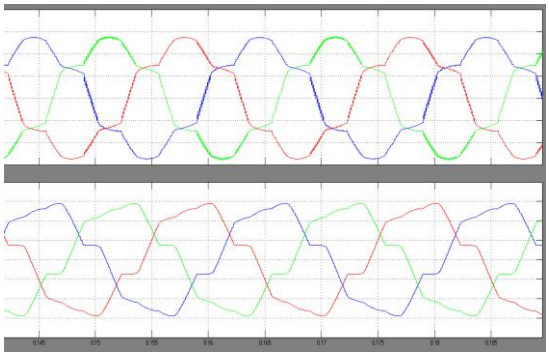

Fig. 7. Before compensation. (a) Terminal voltages. (b) Source currents.

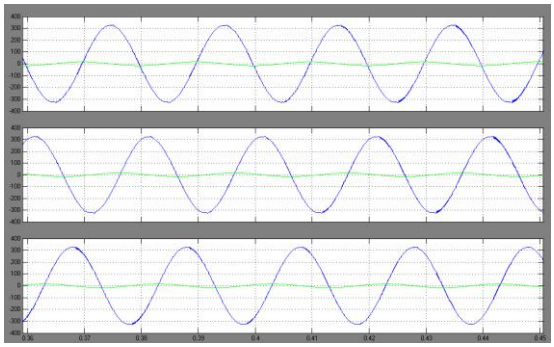

Fig. 8. Terminal voltages and source currents using the traditional method. (a) Phase- . (b) Phase- . (c) Phase- .

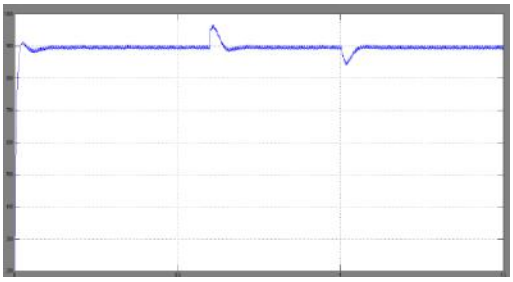

Fig. 9. (a) Voltage at the dc bus.

shows the dc bus voltage regulated at a nominal voltage of 1300 V. Fig. 9 shows the load angle settled around 8.50 . Using the proposed method, terminal voltages and source currents in phases, , and are shown in Fig. 10(a)–(c), respectively. It can be seen that the respective terminal voltages and source currents are in phase with each other, in addition to being balanced and sinusoidal. Therefore, UPF is achieved at the load terminal. For the considered system, waveforms of load reactive power (Ql), compensator reactive power (Qc), and reactive power at the PCC (Qpcc) in the traditional and proposed

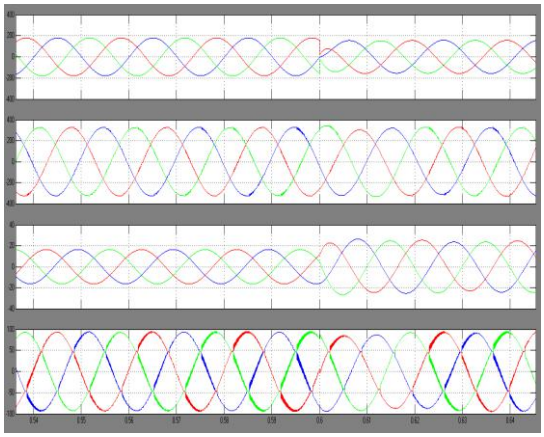

Fig. 10. Terminal voltages and source currents using the proposed method.

In the traditional method, the compensator needs to overcome voltage drop across the feeder by supplying reactive power into the source. As shown in Fig.11, reactive power that is supplied by the compensator and has a value of 4.7 kVAr is significantly more than the load reactive power demand of 2.8 kVAr. This additional reactive power of 1.9 kVAr goes into the source.

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This confirms that significant reactive current flows along the feeder in the traditional method. However, in the proposed method, UPF is achieved at the PCC by maintaining suitable voltage magnitude. Thus, the reactive power supplied by the compensator is the same as that of the load reactive power demand. Consequently, reactive power exchanged by the source at the PCC is zero. These waveforms are given in Fig. 11. Fig. 12(a) and (b) shows the source rms currents in phase for the traditional and proposed methods, respectively. The source current has

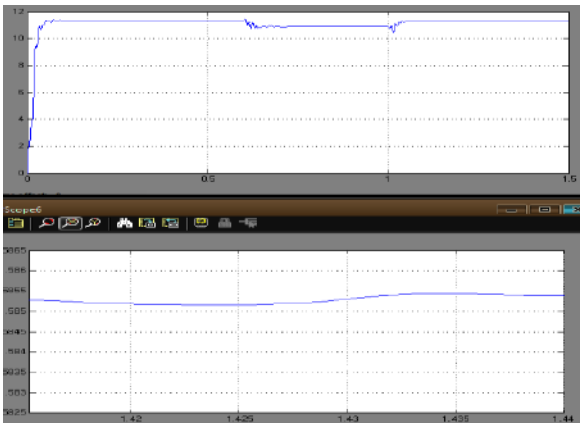

Fig. 11. Phase- source rms currents. (a) Traditional method. (b) Proposed method.

decreased from 11.35 to 10.5 A in the proposed method. Consequently, it reduces the ohmic losses in the feeder. Fig. 12(a) and (b) shows the compensator rms currents in phase- for the traditional and proposed methods, respectively. The current has decreased from 8.4 to 5.2 A in the proposed method. Losses in the VSI represented by resistance and rating of VSI are defined as follows:

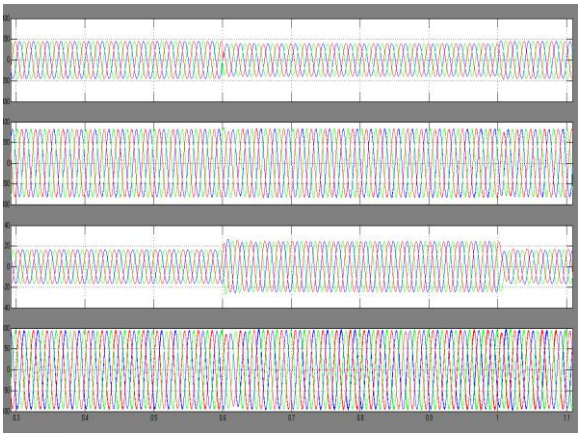

Fig12 (a) Source voltages. (b) Terminal voltages. (c) Voltage at the dc bus. (d) Compensator rms current in the proposed method.

CONCLUSION

This paper proposes another calculation to create reference voltage for a dissemination static compensator (DSTATCOM) working in voltage-control mode. The proposed plan displays a few points of interest contrasted with customary voltage-controlled DSTATCOM where the reference voltage is subjectively taken as 1.0 p.u. The proposed plan guarantees that solidarity force variable (UPF) is accomplished at the heap terminal amid ostensible operation, which is unrealistic in the conventional strategy. Likewise, the compensator infuses lower streams and, subsequently, lessens misfortunes in the feeder and voltage-source inverter. Further, a sparing in the rating of DSTATCOM is accomplished which expands its ability to moderate voltage list. About UPF is kept up, while managing voltage at the heap terminal, amid burden change. The state-space model of DSTATCOM is joined with the miscreant prescient controller for quick load voltage regulation amid voltage aggravations. With these elements, this plan permits DSTATCOM to handle power-quality issues by giving force element amendment, consonant disposal, burden adjusting, and voltage regulation taking into account the heap prerequisite. Reproduction and exploratory results are introduced to exhibit the adequacy of the proposed calculation.

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