Trends in Engineering and Technology (NCTET-2K17)
International Journal of Advanced Engineering Research and Science (IJAERS) *Special Issue-5*
https://dx.doi.org/10.22161/ijaers/nctet.2017.eee.20 *ISSN: 2349-6495(P) | 2456-1908(O)*

A NEW CONTROL TOPOLOGY OF A CASCADED MULTILEVEL INVERTER FOR SOLAR APPLICATIONS

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Abstract- *Solar energy is one of the renewable energy which is used to generate electricity with the help of PV arrays. DC-DC converter is used to step up the DC voltage from PV arrays and then it is connected to an inverter for AC applications. Conventional inverters have many issues like non sinusoidal output, high total harmonic distortion (THD), high switching stress and more number of switches. So multilevel inverter (MLI) have gained much importance over conventional inverters for high voltage and high power applications, due to the increased number of voltage levels producing less number of harmonics. In this paper, a cascaded asymmetric multilevel inverter is proposed which contains minimum number of switches and can be employed in AC applications using solar energy. The proposed topology consists of 25 output levels using 10 switches with near sinusoidal output, thereby reducing gate driver circuitry and optimizing circuit layout. Asymmetric multilevel inverter is more advantageous than symmetric multilevel inverter in obtaining more number of output levels using same number of voltage sources. The other advantages of proposed topology are low voltage stress and reduced THD. The THD for proposed inverter circuit is only 4.98%. Modeling and simulation is carried out using MA TLAB/SIMULINK.*

Index Terms— Renewable Energy; Multilevel Inverter; Total Harmonic Distortion; Cascaded Asymmetric.

I. INTRODUCTION

Multilevel converters have received more and more attention because of their capability of high voltage operation, high efficiency, and low electromagnetic interference (EMI). The desired output of a multilevel converter is synthesized by several sources of dc voltages. With an increasing number of dc voltage sources, the converter voltage output waveform approaches a nearly sinusoidal waveform while using a fundamental frequency switching scheme. This results in low switching losses, and because of several dc sources, the switches experience a lower. As a result, multilevel converter technology is promising for high power electric devices such as utility applications.

For these applications, the output voltage of the converters must meet maximum total harmonic distortion (THD) limitations; some kind of method must be used to control the harmonics. The traditional PWM method, space vector pulse-width modulation (PWM) method, sub-harmonic PWM method (SH-PWM), and switching frequency optimal PWM (SFO-PWM) for multilevel converters require equal dc voltage sources. For fundamental switching scheme, the transcendental equations characterizing the harmonic content can be converted into polynomial equations. Elimination theory has been employed to determine the switching angles to eliminate specific harmonics, such as the fifth, seventh, 11th, and the 13th.

However, as the number of dc sources increases, the degrees of the polynomials in these equations are large and one reaches the limitations of contemporary computer algebra software tools (e.g., Mathematic or Maple) to solve the system of polynomial equations using resultants. Another method to eliminate harmonics in multilevel inverters is highlighted. The multilevel converter is a promising power electronics topology for high power motor drive applications because of its low electromagnetic interference (EMI) and high efficiency using a fundamental switching scheme.

The cascaded multilevel converter with separate DC sources can fit many of the needs of all-electric vehicles because it can use onboard batteries or fuel cells to generate a nearly sinusoidal voltage waveform to drive the main vehicle traction motor. Traditionally, each phase of a cascaded multilevel converter requires n DC sources for $2n + 1$ level.

For many applications, to get many separate DC sources is difficult, and too many DC sources will require many long cables and could lead to voltage unbalance among the DC sources. To reduce the number of DC sources required when the cascaded H-bridge multilevel converter is applied to a motor drive, a scheme is proposed in this paper that allows the use of a single DC source (such as battery or fuel cell) as the first DC source with the remaining $n-1$ DC sources being capacitors in the cascaded H bridges multilevel converter.

The control goal here is to maintain the balance of the DC voltage level of each of the capacitors while simultaneously producing a nearly sinusoidal three-phase output voltage with a low switching frequency control method. However, one disadvantage of the hybrid cascaded multilevel converter is that it has narrow modulation index range when using fundamental frequency switching scheme at high modulation index,

https://dx.doi.org/10.22161/ijaers/nctet.2017.eee.20 *ISSN: 2349-6495(P) | 2456-1908(O)*

and this disadvantage limits its highest output voltage when maintaining the capacitors' voltages.

To conquer this problem, this paper proposes a modulation extension control algorithm to extend the modulation index range for hybrid cascaded H-bridge multilevel converters. The reason for narrow modulation index range is from longer discharging time and shorter charging time when the hybrid cascaded multilevel converter outputs high voltages.

Multilevel inverters include diode clamped converter, flying capacitors, cascaded and H-bridge MLI. This MLI help to achieve near sinusoidal output waveforms with reduced THO. As the number of output levels increase, harmonics decrease. The disadvantage of conventional MLI is that if more number of output levels is required, then more number of components is needed and due to this complexity increases in gate driver circuits. At present the most famous hardware implementable topologies are cascaded H-bridge and the diode clamped. The drawback of symmetric MLI can be overcome by asymmetric MLI. In this paper a novel cascaded asymmetric MLI topology is proposed which requires minimum number of switches with reduced THD.

II. PROPOSED METHOD

The proposed topology contains minimum number of switches for generating same output levels as compared to conventional MLI. The proposed MLI's basic cell generates 5 output levels using 2 voltage sources (here the voltage sources represent stepped up DC-output voltage from PV arrays) and 5 switches with anti-parallel diodes. Fig.1 shows the arrangement of these switches, where SII, SI2, SI3, SI4 are arranged same as conventional H-bridge while S 15 is added to increase output level by selecting appropriate voltage source.

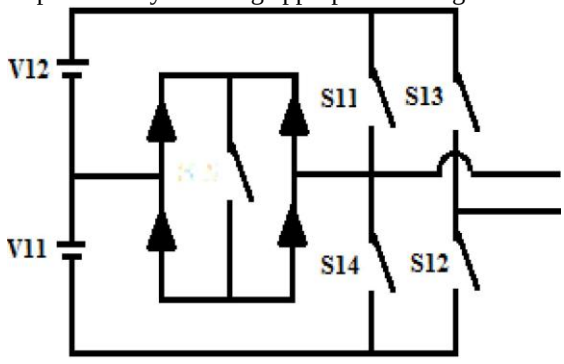

Fig.1 Basic Cell of proposed MLI

The TABLE-I is shown below, regarding switching states of proposed MLI's basic cell where logic' l' is considered as 'ON' state and logic' 0' is considered as' OFF' state of switch. The basic cell consists of 2 voltage sources.

TABLE-I
SWITCHING STATES OF BASIC CELL

S11	S12	S13	S14	S15	Vol (o/p volt.)
1	1	0	0	0	V11+V12
0	1	0	0	1	V11
0	1	0	1	0	0
1	0	1	0	0	
0	0	1	0	1	-V12
0	0	1	1	0	- (V11+V12)

When the number of voltage sources in basic cell increase, then the number of output levels also increase. The proposed topology of multilevel inverter is employed by cascaded arrangement of two basic cells. Here the Fig.2 shows MLI where 25 output levels are obtained by using only 10 switches. This arrangement can be further augmented by cascading' P' number of basic cells in series. As the number of output levels is increased the output approaches close to sinusoidal waveform. This topology contains two cascaded basic cells. Each cell consists of two equal voltage sources. The voltage sources of second basic cell are in ratio of l:5 with respect to voltage sources of first basic cell. This topology helps to generate 25 output levels. This arrangement is defined as asymmetric MLI because of unequal voltage sources in two respective basic cells. Similarly if voltage sources of P cascaded cells are equal to the voltage sources of other basic cells that is in l: 1 ratio then the arrangement is defined as symmetric MLI.

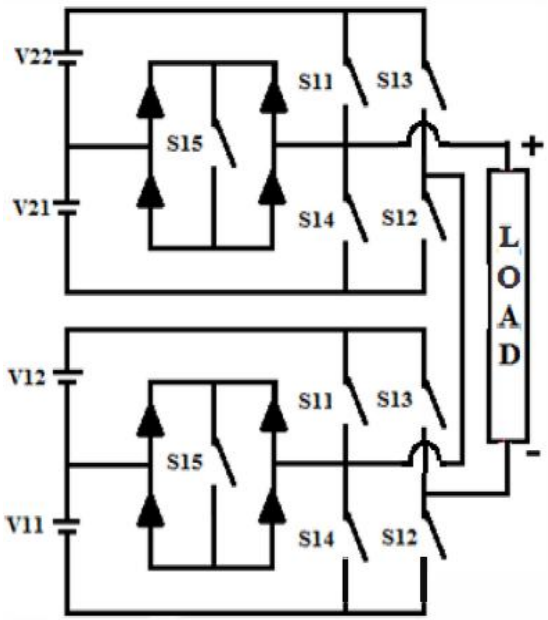

Fig.2 Proposed MLI with 10 switches

The diodes are arranged as shown in the Fig.2. Total number of diodes for one basic cell is 4. So if 'P' cascaded basic cells are used then the total number of diodes required is given by 4P (anti-parallel diodes across switch are not considered). Here in proposed topology total 8 diodes are used. Zero output voltage is represented with two switching states. Switches SIS and S25 are

https://dx.doi.org/10.22161/ijaers/nctet.2017.eee.20 *ISSN: 2349-6495(P) | 2456-1908(O)*

select switches of two respective basic cells. These switches help to add number of output levels. When all basic cells are cascaded in series, output voltages of each basic cell are added together to achieve final output voltage across MLI.

III. SIMULATION RESULTS

The simulation for proposed topology is done using 10 switches and the voltage sources in second basic cell are equal to each other but in 1:5 ratios with voltage sources in first basic cell. FFT window is used for harmonic spectrum analysis in MATLAB/ SIMULINK.

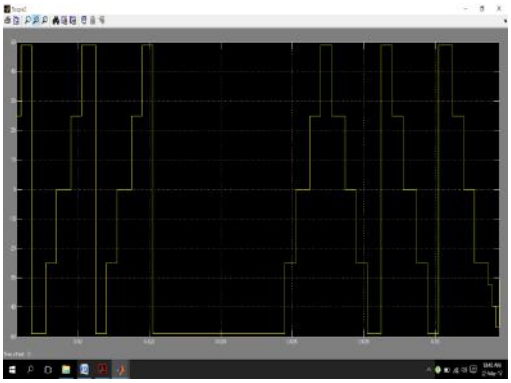

Fig:3(a)

Fig:3(b)

Fig:3 (a) & (b) output voltage of first and second basic cells respectively.

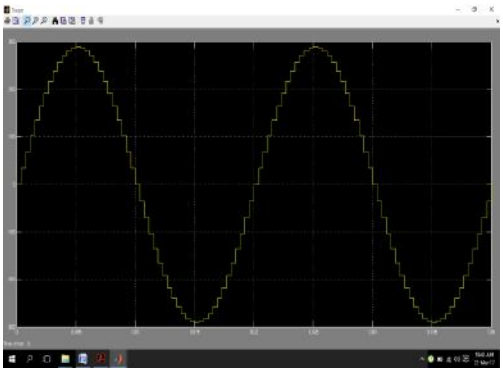

Fig:4(a)

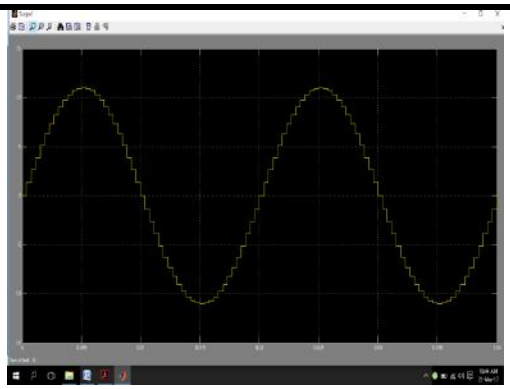

Fig:4(b)

Fig:- 4 25 level output waveform MLI using 10 switches for R load.

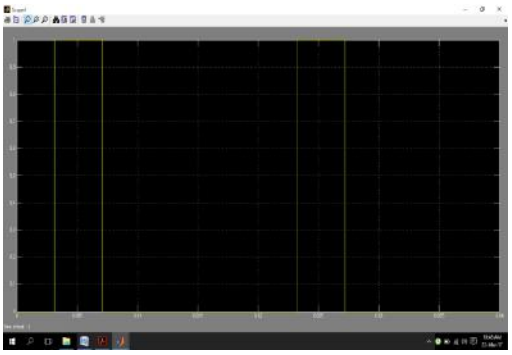

Fig:5(a)

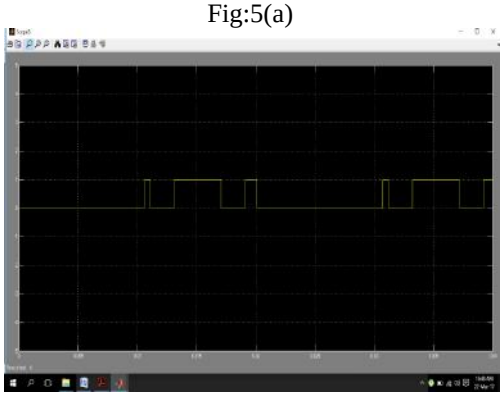

Fig:5(b)

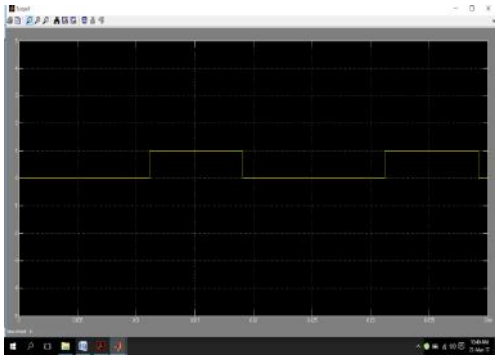

Fig:5(c)

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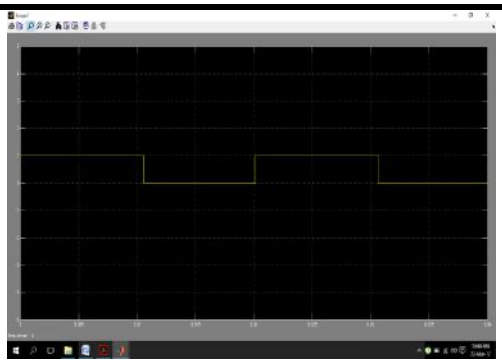

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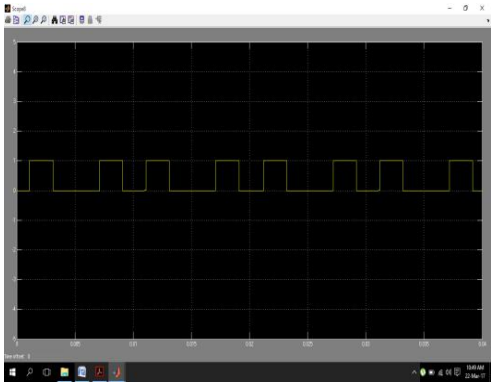

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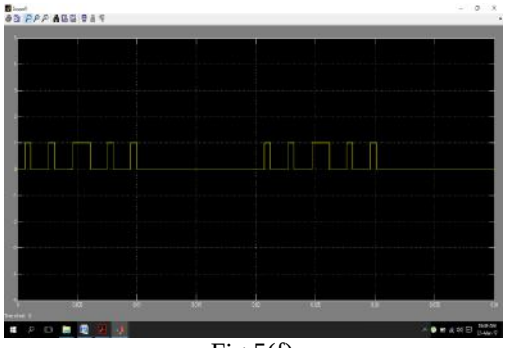

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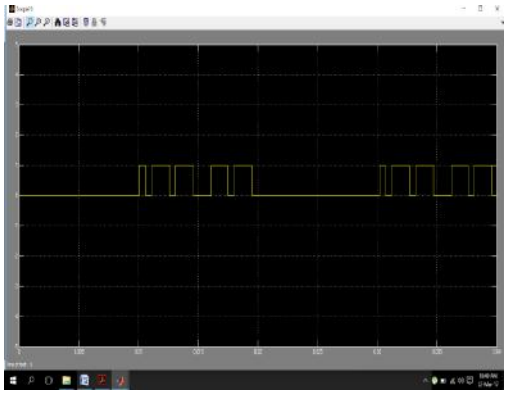

Fig:5(g)

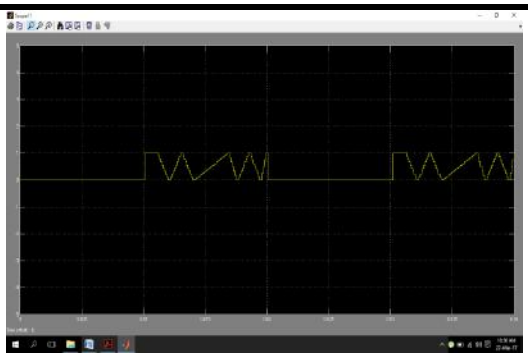

Fig:5(h)

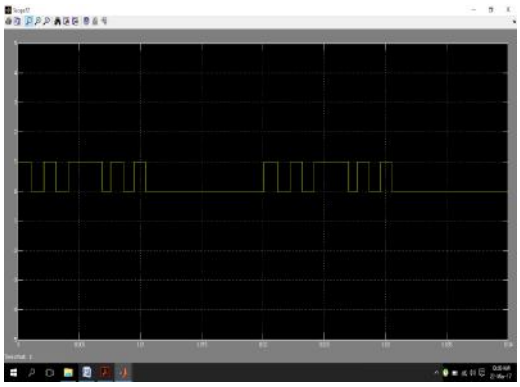

Fig:5(i)

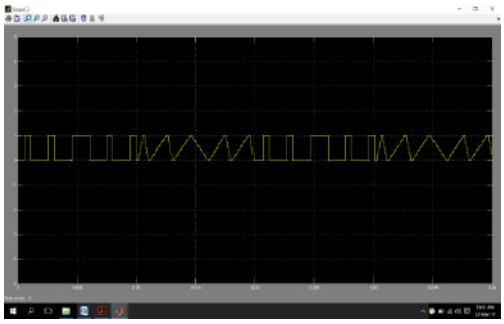

Fig:5(j)

Fig:5 switching stress across each switch.

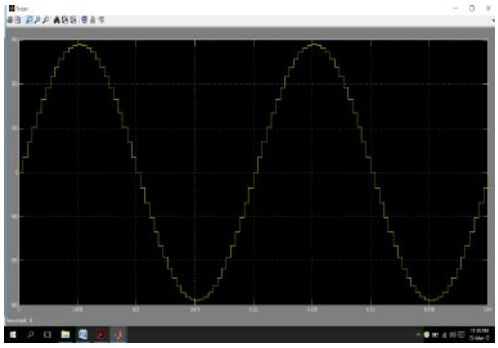

Fig:6 (a)

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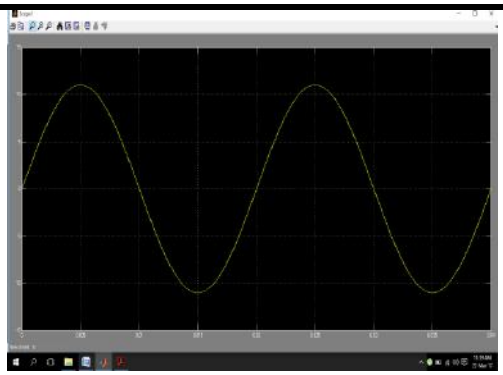


Fig:6 (b)

Fig:6 25 level output waveform MLI using 10 switches for RL load.

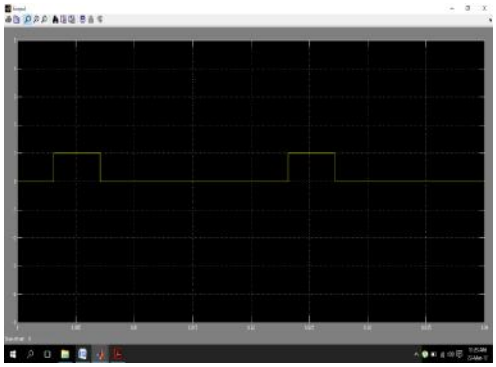


Fig:7(a)

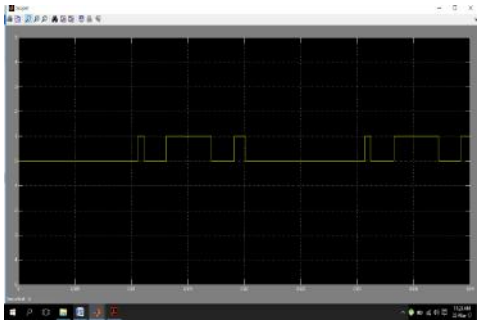


Fig:7(b)

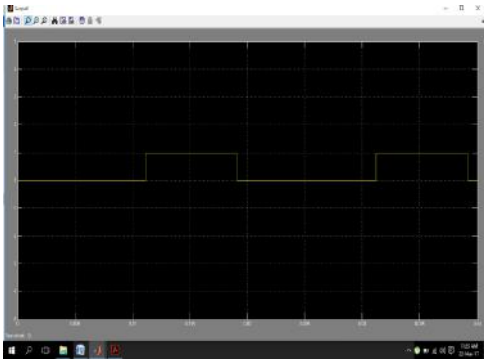


Fig:7(c)

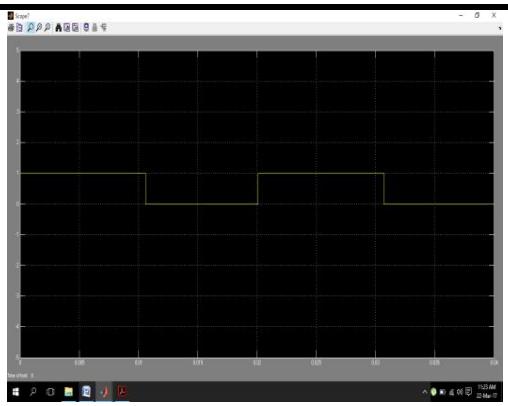
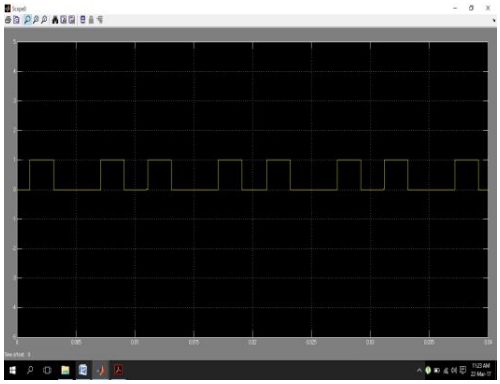


Fig:7(d)



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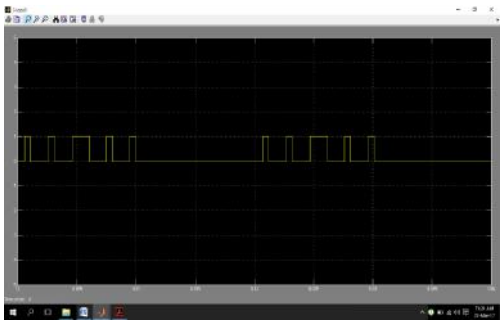

Fig:7(f)

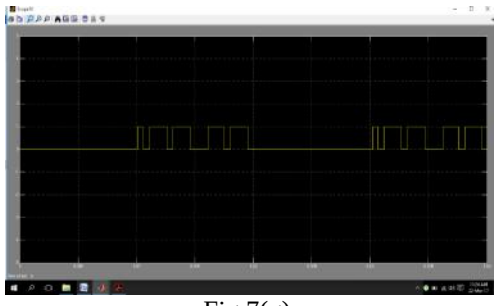

Fig:7(g)

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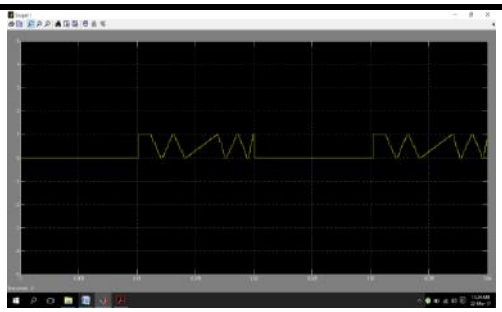
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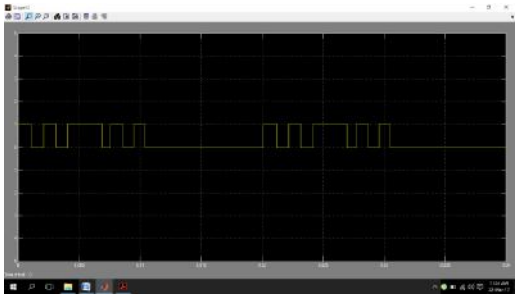
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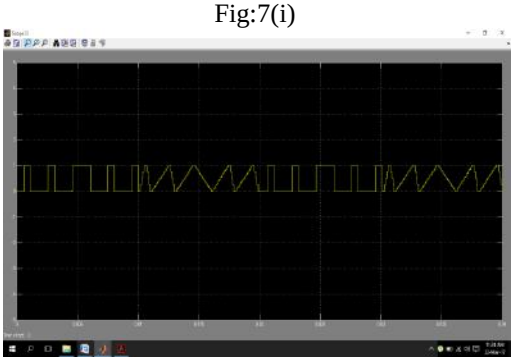
Fig:7(j)

Fig:7 switching stress across each switch.

The below figure shows the SIMULINK model of extension of MLI with 10 switches. In this we place the filters at the load side. Switching states of switches, output voltage of each cell, output waveforms using R-Ioad and RL load, switching stress across each switch and THD are shown in figures respectively. The main advantage is that output is almost near-sinusoidal waveform.

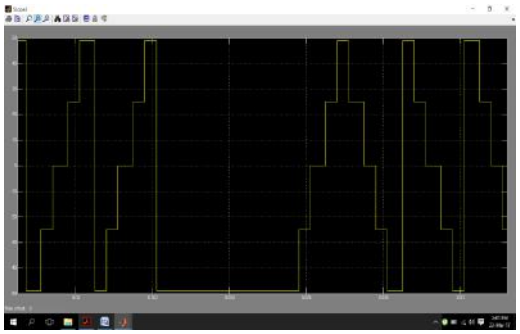
Fig:8 (a)

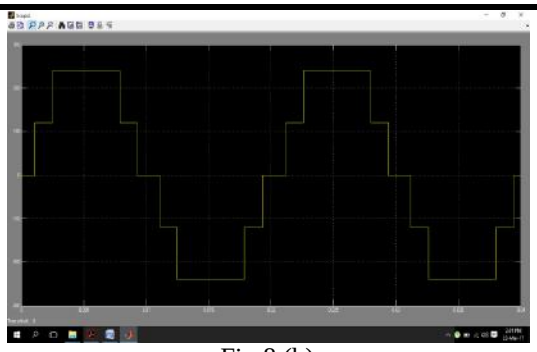
Fig:8 (b)

Fig:8 (a) & (b) output voltage of first and second basic cells respectively.

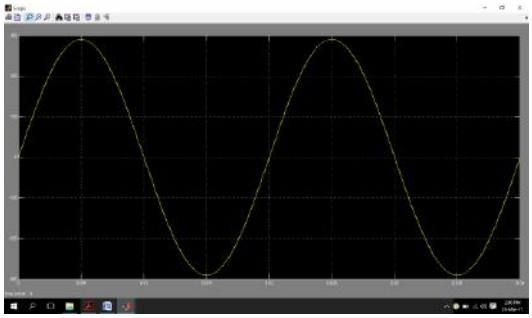
Fig:9 (a)

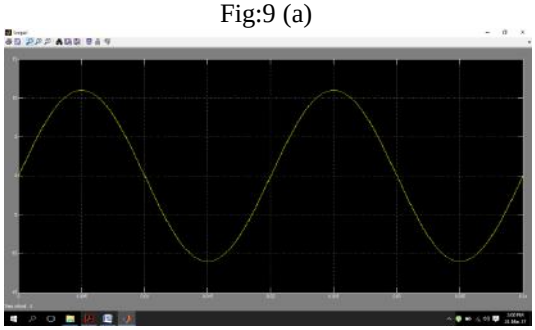
Fig:9 (b)

Fig:9 25 level output waveform MLI using 10 switches for R load.

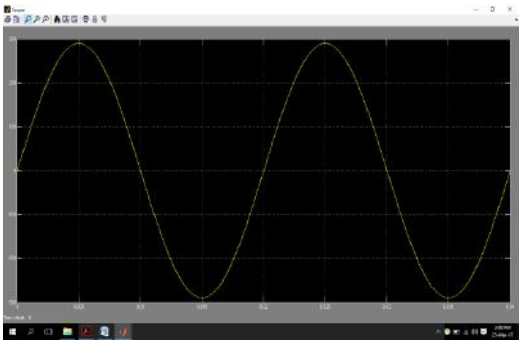
Fig:10 (a)

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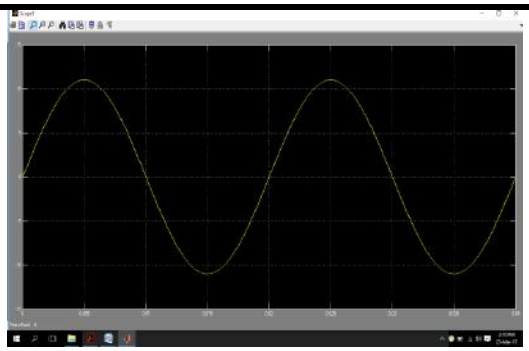

Fig:10 (b)

Fig:10 25 level output waveform MLI using 10 switches for RL load.

IV. CONCLUSION

In this paper, a cascaded multilevel inverter is proposed which requires minimum number of switches with increased output levels where, output waveform is near-sinusoidal. Compared with conventional multilevel inverters, it requires less number of components to achieve same number of output levels. Overall THD is very low and thus the quality of output waveform is improved. Also this asymmetric multilevel inverter is more advantageous over symmetric multilevel inverter using same number of switches, for producing more number of output levels. Due to the use of fewer switches, optimized circuit layout and packaging is possible. Thus less cost is required to implement the proposed inverter. When sinusoidal pulse width modulation (SPWM) technique is installed THD value will reduce even further. This topology can be successfully installed for solar based ac applications.

V. REFERENCES

[1] J .Rodriguez, S. Bernet, B. Wu, J.O. Pontt, and S .Kouro, "Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives," IEEE Transactions on Industrial Electronics" vo1.54, no.6, pp.2930-2945, Dec. 2007.

[2] Wei Zhao, Hyuntae Choi, G. Konstantinou, M. Ciobotaru and V. G. Agelidis "Cascaded H-bridge Multilevel Converter for Large-scale PV Grid-Integration with Isolated DC-DC stage" PEDG, IEEE 2012.

[3] S. Rivera, S. Kouro, B. Wu, 1. 1. Leon, 1. Rodriguez and L. G. Franquelo "Cascaded H-bridge multilevel converter multi string topology for large scale photovoltaic systems," IEEE ISlE 2011, pp.1 837-1844.

[4] N.A. Rahim, K. Chaniago, and 1. Selvaraj "Single-Phase Seven-Level Grid Connected Inverter for Photovoltaic System", IEEE Transactions on Industrial Electronics, Vol. 58, No. 6, June 2011, pp. 2435-2443.

[5] A Nordvall, "Multilevel Inverter Topology Survey", M.S Thesis in Electric Power Engineering, Department of Energy and Environment, Chalmers University Techonology, Goteberg, Sweden, 2011.

[6] F.Z. Peng, , W. Qian, and D. Cao, "Recent advances in multilevel converter inverter topologies and applications," 2010 International Power Electronics Conference (lPEC), pp.492-501, 21-24, June 2010

[7] 1. Rodriguez, 1.S.Lai, and F.Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. on Industrial electronics, vol. 49, no. 4, pp. 724-738, Aug. 2002.

[8] Z. Du, I.. M. Tolbert, B. Ozpineci, and K. N. Chiasson, "Fundamental frequency switching strategies of a seven-level hybrid cascaded H bridge multilevel inverter," IEEE Trans. Power Electron., vol. 24, Kan. 2009.

[9] S. Kouro, M.Malinowski, K. Gopakumar, J. Pou,L. Franquelo, B. Wu, J. Rodriguez, M. Pe' andrez, and 1. Leon, "Recent advances and industrial applications of multilevel converters," IEEE Transactions on Industrial Electronics, vol. 57, pp. 2553 -2580, Aug. 2010.